Verifying Interoperability and Application Performance of PMUs and PMU-enabled IEDs

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***Abstract*—This paper presents a new test methodology for verifying the interoperability and application performance of PMUs and PMU-enabled IEDs at the device and system level. Two types of tests are defined to evaluate the performance of synchrophasor devices from two different aspects: design and application. The interoperability between PMUs, time synchronization options, and phasor data concentrators (PDCs) can be verified by design test methodology. A fault location algorithm using two-end synchronized measurements is used to evaluate the application performance. A reference PMU algorithm and synchrophasor system test set-up have been developed to perform the tests. Nine commercial PMUs and four GPS receivers with different synchronization options are selected to perform the tests. The test results are summarized at the end.**

***Index Terms*—phasor measurement unit (PMU), synchronized phasor, power grid, phasor estimation, intelligent electronic device (IED), fault location**

I. Introduction

THE use of synchronized measurements, particularly synchrophasors, has a history of over thirty years of research and development. In the last few years the effort of deploying and demonstrating variety of applications that can benefit from synchronized measurements has been accelerated through the DOE funding under American Recovery and reinvestment Act (ARRA) and coordinated by the North American Synchrophasor Initiative (NASPI) and other related industry efforts. Most recently several utilities and regional market operators have developed plans for large scale deployment of such a technology. New applications using synchronized data will become an important part of the overall power system operation [1]-[7].

The deployment of the Intelligent Electronic Devices (IEDs) for substation synchronized measurement applications has two approaches: a) use of Phasor Measurement Units-PMUs (dedicated high precision recording instruments), and b) use of PMU-enabled IEDs (Digital Fault Recorders-DFRs, Digital Protective Relays-DPRs, Digital Disturbance Recorders-DDRs, etc. that have PMU measurement capability). The number of installed units in the US power grid will pretty soon go over 1000 with even more to be installed in the next 5-10 years. The total cost of the overall solution may exceed the cost of individual recording devices by several orders of magnitude. With installation of such costly infrastructure the risks of the asset becoming stranded are real and mitigating measures need to be put in place to avoid such an undesirable outcome. The risk is exuberated by the following integration features used today:

- Multi-vendor PMUs and PMU-enabled IEDs with proprietary features;
- Various Time synchronization options;
- Mixed type of PDCs and communication networks.

The mitigation of risk requires reliance on the standards and appropriate testing to ensure compliance and consistency across multiple IED types. This will assure future scalability, upgradeability, and interoperability hence avoiding the costly infrastructure becoming a stranded asset.

IEEE C37.118-2005 standard defines synchrophasor measurements used in the power system applications [8]. The dynamic performance requirements are captured in IEEE C37.118.1-2011 [9].The Performance and Standards Task Team (PSTT) of the North American Synchrophasor Initiative (NASPI) issued a PMU system testing and calibration guide [10]. The communication requirements for PMUs are defined in IEEE C37.118.2-2011.

While many efforts have been focused on testing individual PMUs [11]-[22], the tests did not address application performance assessment of PMU-enabled IEDs and interoperability tests for system solutions consisting of many diverse types of the IEDs, time synchronization methods, communication options and PDCs.

This paper discuses test classification first, and then focuses on reference PMU algorithm and test implementation next. Test results and conclusions are given at the end.

II. Test Classification

In this section, two types of tests, namely design and application test are defined to evaluate the synchrophasor devices from the aspects of how well the device meets standard specification and how well it performs in the use for various applications.

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A. Design Test

The design tests are aimed at verifying the conformance and interoperability compliance of PMUs and PMU-enabled IEDs, time synchronization methods and PDCs against standards. The conformance performance under specific test conditions is evaluated by comparing the total vector error (TVE), amplitude, phase angle, frequency, and rate of change of frequency (ROCOF) measurements to corresponding theoretical values defined in the standrads. The test conditions including steady state and dynamic state are consistent with those defined in C37.118-2005 [8] and C37.118.1-2011 [9]. The interoperability compliance performance between synchrophasor devices, such as time clock and PMU, PMU and PDC, is verified by interchanging equivalent parts of the system solution. The performance is measured by comparing the numerical indices against requirements defined in standards. The mathematical signal models used to create test signals for steady and dynamic states are given in Table I.

The conformance test is performed according to the conditions and scenarios specified in aforementioned standards. The performance of PMUs and PMU-enabled IEDs is accessed against the numerical criteria.

The interoperability between synchrophasor devices, including the PMU, time synchronization device and PDC, is verified by interchanging equivalent parts in the system solution, as described in Table II. The time synchronization includes the use of GPS receivers with IRIG-B / PPS options and transfer of synchronization signals using IEEE 1588/IEEE 238 communication protocols [23], [24]. The phasor data concentrator (PDC) includes both software (PC-based) and hardware (standalone) solutions. The performance is measured by the numerical results against specification defined in standards or applications. In terms of the type of time source, we categorize PMUs into three classes: a. Direct use of GPS signalobtained through built-in GPS receiver; b. IRIG-B input, which requires external time synchronization source; c. IEEE 1588 transfer of synchronization signal, which is achieved through communication network. Some PMUs may have all the three features. The selected steady-state and dynamic state tests are performed for each combination to generate the numerical results. The test conditions are consistent so that the test results are comparable.

B. Application Test

The application tests are aimed at verifying performances of specific applications, i.e. fault location, state estimation, etc. this is done under variations of the use of different PMUs, time synchronization options, PDCs and communication protocols. A fault location algorithm using two-end synchronized measurements is selected to perform the application test [25].

TABLE I
TEST SIGNAL MODELS

Test Type		Signal Model
Steady state		$x(t) = X_m\cos(2\pi ft + \varphi)$ X_m: amplitude, φ: initial angle, f: frequency
Dynamic	Modulation	$x(t) = X_m[1 + k_x\cos(2\pi f_m t)]$ $\cdot \cos[2\pi f_0 + k_a\cos(2\pi f_m t - \pi)]$ k_x, k_a : amplitude, phase modulation factor f_m: modulation frequency
	Step change	$x(t) = X_m[1 + k_x u(t)]$ $\cdot \cos[2\pi f_0 t + k_a u(t)]$ $u(t)$: unit step function k_x, k_a : amplitude, phase step factor
	Frequency ramp	$x(t) = X_m\cos(2\pi f_0 t + \pi f_d t^2 + \varphi)$ f_0: nominal frequency f_d: frequency changing rate

TABLE II
TEST DESCRIPTION FOR INTEROPERABILITY VERIFICATION

Target	Configuration	Test Item
Interoperability between the Time clock and PMU or PMU-enabled IED	Direct GPS	Steady state and Dynamic state test scenarios
	IRIG-B / PPS	
	IEEE 1588 v2 PTP	
Interoperability between the PMU or PMU-enabled IED and PDC	Software PDCs	
	Hardware PDCs	

Fig. 1 shows a one-line diagram and equivalent circuit when a fault occurs on a transmission line. From the equivalent circuit diagram, we have two equations:

$$\dot{V}_S = xZ_L \cdot \dot{I}_S + \dot{V}_f \tag{1}$$

$$\dot{V}_R = (1-x)Z_L \cdot \dot{I}_R + \dot{V}_f \tag{2}$$

Subtracting (1) from (2) to eliminate $\dot{V}_f$, we obtain the equation for computing location x using two-terminal voltage and current measurements:

$$x = \frac{\dot{V}_S - \dot{V}_R + Z_L \cdot \dot{I}_R}{Z_L(\dot{I}_S + \dot{I}_R)} \tag{3}$$

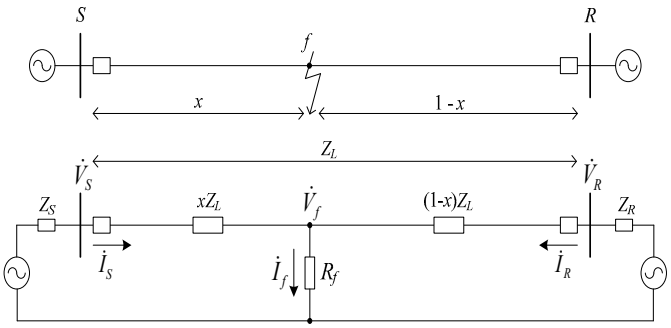

Fig. 1. One-line diagram and equivalent circuit for a fault on transmission line

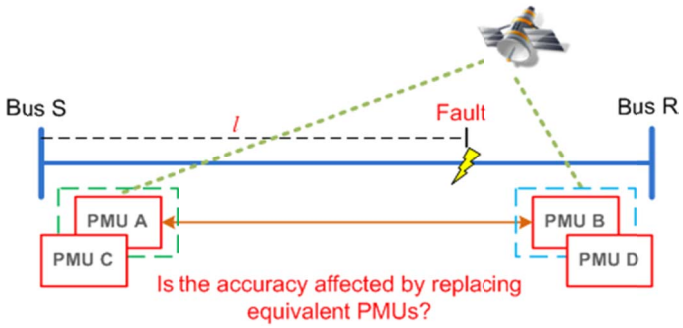

Fig. 2. Various PMU options utilized at two ends

TABLE III
FAULT SCENARIOS FOR APPLICATION TEST

Target	Configuration	Fault Variation
PMU or PMU-enabled IED	Reference time clock, no PDC connected	Location: 10%,50%, 90%; Type: SLG, LL, LLG, 3L; Inception: 0˚, 45˚, 90˚; Resistant: 0Ω, 25Ω, 50Ω.
Time synchronization method	Reference PMU, no PDC connected	
PDC and communication medium	Reference time clock and reference PMU	

The synchrophasor based fault location algorithm, as described above, is selected to investigate how interchanging different PMUs and PMU-enabled IEDs, time synchronization methods, PDCs and communication protocols affect the application performance. Fig. 2 shows an example of exchanging equivalent PMUs at two ends. The three elements of the system solution are tested individually. The performance is evaluated by comparing the distance calculated using phasor measurements from PMUs under test to the value calculated using reference values.

The fault disturbances variations may be various fault properties: type, location, inception angle and fault resistance. The test scenarios are summarized in Table III. We use transient voltages and currents generated from the ATP/EMTP system developed for testing [26]. A 230 kV power network created by IEEE Power Engineering Society's Power System Relaying Committee (PSRC) is used for performing fault simulations [27]. The files recording voltage and current waveforms are read and fed to test system. The power network modeled in ATP is given in Fig.3.

III. REFERENCE PMU ALGORITHM

A. Phasor Estimation Algorithm

The reference algorithm for estimating phasors is described in this section. It is derived based on a dynamic signal model and uses a quadratic form to handle the changing parameters. For real-time application, this algorithm can achieve very good accuracy against the requirements specified in the standards. For testing, because the frequency variable of a test signal is known, instead of using the estimated frequency, we use the true value of a test signal's frequency to achieve higher accuracy.

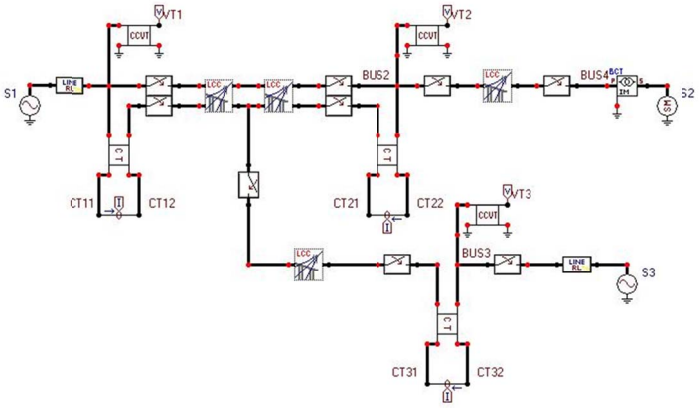

Fig. 3. Power network defined by PSRC modeled in ATP/EMTP

We use constant sampling frequency ($_s$ = 50 kHz) to sample the input voltage and current signals. The size of data window for estimating phasor is one cycle period of the nominal frequency, i.e. the number of samples within a data window is 50000/60 ≈ 833. Let F_s be the PMU reporting rate (frame per second). For some reporting rate, the output interval is not an integer, for example, F_s = 30/s, the output interval is 50000/30 = 1666.67. In this case the phase compensation is performed using equation (4) as follows:

$$\Delta\varphi = 2\pi f \cdot [1/F_s - \text{round}(f_s/F_s)/f_s] \quad (4)$$

where f is the frequency of input signals. Fig. 4 illustrates the compensation scheme. It should be noted that the phase compensation is unnecessary for the measurement at each integer second, i.e. pulse per second (pps).

An example of performing the conformance test on PMUs and PMU-enabled IEDs using the reference PMU is shown in Fig. 5. This test system includes a test signal generator, reference time clock with 30ns RMS (corresponding to 0.0012% TVE), and an error analyzer. The PMU under test and reference PMU observe the same voltage and current signals, thus the uncertainty caused by the signal generator can be neglected. The accuracy of the entire test system depends on the accuracy of the phasor estimation algorithm, time clock and data acquisition system. The data acquisition has an uncertainty of less than 0.0015% TVE [28].

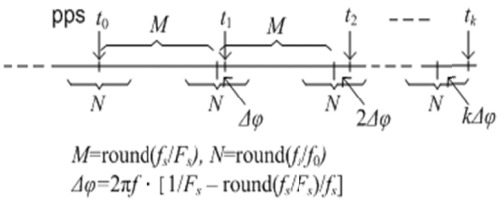

Fig. 4. Phase angle compensation for estimated phasors

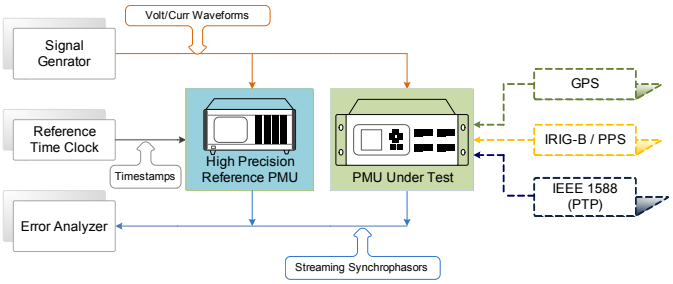

Fig. 5. Phase Diagram for performing conformance tests

TABLE IV
RESULTS OF REFERENCE ALGORITHM ACCURACY STUDY

Test Type		Performance	Max TVE (%)
Steady state		Class P	8.3-e12
		Class M	1.2-e11
Dynamic	Modulation	Class P	7.8-e04
		Class M	0.08
	Frequency ramp	Class P	1.3-e07
		Class M	1.6-e05

B. *Accuracy Study*

The accuracy study for the reference algorithm has been performed using the signals given in Table I, which include the signal models representing steady state and dynamic state conditions in power system. The frequency and rate of change of frequency have high accuracy because the real value is used. The maximum TVEs are recorded in Table IV. One can refer to reference [12] for the step test approach. Combining the uncertainties of phase estimation algorithm, time clock and DAQ, the overall testing system has an uncertainty of less than 0.08% TVE.

IV. TEST IMPLEMENTATION

The design and application tests are performed using a well developed laboratory system for synchrophasor testing. The photo of the system is shown in Fig. 6. It consists of a GPS receiver used to synchronize the system to UTC, a signal acquisition system used to generate and sample test signals up to 500 kHz, three voltage and current amplifiers connected to PMUs and PMU enabled IEDs providing test signals at both typical and small voltage levels, three voltage attenuators and three current shunts. GPS signal, IRIG-B and IEEE 1588 v2 are available for various synchrophasor devices. A series of software models is developed in LabVIEW [29] for automating test procedures and analyzing test results.

Fig. 7 shows the architecture of the synchrophasor test system. Each module of the system is described as follows:

- Time synchronization options – provides reference UTC time sources to device under test. The options include direct GPS signal, IRIG-B and IEEE 1588 PTP.

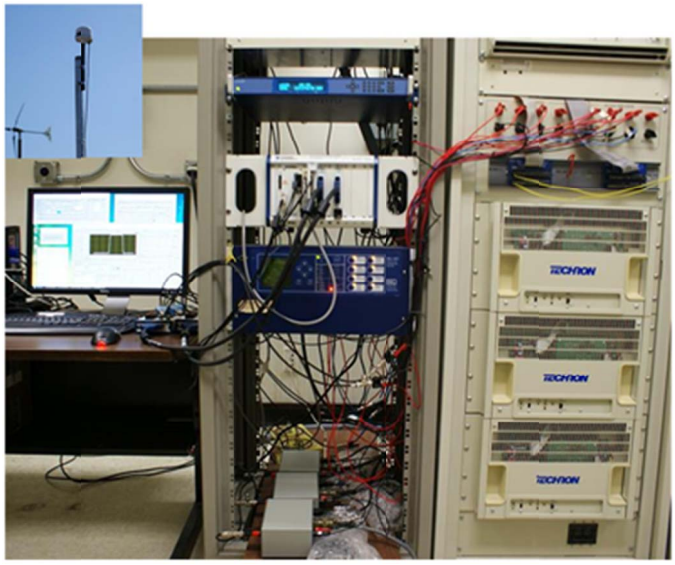

Fig. 6. Synchrophasor test and calibration system

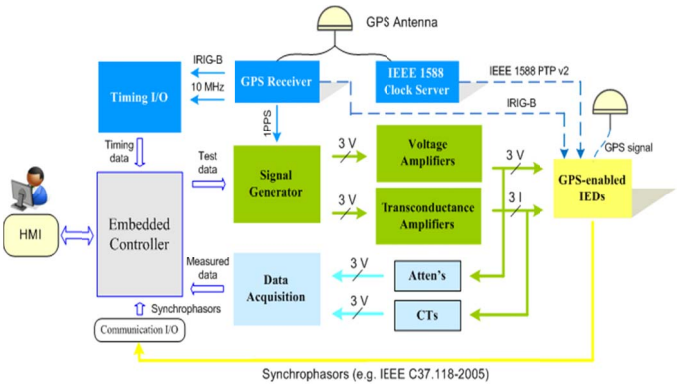

Fig. 7. Synchrophasor test system architecture

- Data acquisition system – converts digital test signals to analog signals as inputs to amplifiers or synchrophasor units with low-voltage interfaces; samples voltage and current signals for phasor estimation module.
- Reference signal source and conditioner – provides voltage and current signals at nominal level (voltage: 100 V, current: 5A or 1A); scales high voltage signals down to the low level voltage (≤10 V) for data acquisition system.
- Syncrophasor data interface – provides connection and data transfer for PMUs. The interfaces include serial port and Ethernet connection.
- Reference PMU – provides reference phasors compared to the phasors measured by device under test. The detailed description is presented in the following section.
- GUI Interface – provides a console for controlling, monitoring and collecting test results.

V. Test Results

Preliminary test results for performing the conformance test, interoperability test and application test are presented in this section. The conformance test results have been reviewed by vendors and their feedback is taken into account.

A. Conformance Test

Nine commercial PMUs and PMU-enabled IEDs from eight different vendors were selected to perform the conformance test. Due to limited number of pages, the configurations for the PMUs, denoted as A – H, are not included. For each test scenario the magnitude error, phasor error, TVE, frequency error and rate of change of frequency error are recorded. The test results are summarized in Table V, in which "S" stands for "satisfied" while "F" stands for "failure", "P" and "M" standard for the class P and class M respectively. From the test results we can see that most PMUs meet the steady state performance requirement, but all of them failed to provide conformance under some dynamic conditions.

B. Interoperability Test

Four types of scenarios are selected to perform interoperability test between PMUs and time synchronization options: the amplitude and frequency variations under steady state, and the modulation and frequency ramp under dynamic state. The test cases are denoted as C1 – C4. We selected four commercial GPS receivers (denoted as Clock A-D) to provide time synchronization signals including IRIG-B and IEEE 1588 v2 PTP. Test results are summarized in Table VI, in which "S" stands for "satisfied", "F" stands for "failure", "N" stands for "Not functional, "P" and "M" standard for the class P and class M respectively. From test results we can conclude that PMU B only works with Clock B; PMU A-1 is unable to provide conformance under condition C1 and C2 when using Clock C; PMU C is unable to provide conformance under condition C3 when using Clock C. In this case we may say that the PMU A-1 and PMU C are not interoperable with Clock C.

TABLE V
CONFORMANCE TEST RESULT SUMMARY

PMU	Class	Steady State Test									Dynamic State Test								
		Magnitude Variation			Phase Angle Variation			Frequency Variation			Measurement Bandwidth			Frequency Ramp			Step Change		
		TVE	FE	RFE	TVE	FE	RFE	TVE	FE	RFE	TVE	FE	RFE	TVE	FE	RFE	RT	DT	MO
PMU A	P	S	S	S	S	S	S	S	S	S	S	**F**	S	S	**F**	**F**	**F**	**F**	**F**
	M	S	S	S	S	S	S	**F**	S	S	S	**F**	S	**F**	**F**	**F**	S	**F**	**F**
PMU A-1	P	S	S	S	S	S	S	S	S	S	S	**F**	S	S	**F**	**F**	**F**	S	**F**
	M	S	S	S	S	S	S	S	S	S	S	**F**	S	S	**F**	**F**	S	S	**F**
PMU B	P	S	S	S	S	S	S	S	S	S	S	**F**	S	S	**F**	**F**	S	**F**	S
	M	S	S	S	S	S	S	S	S	S	**F**	**F**	S	**F**	**F**	**F**	S	**F**	S
PMU C	P	S	S	S	S	S	S	S	S	S	S	**F**	S	S	**F**	**F**	S	S	S
	M	S	S	S	S	S	S	S	S	S	S	S	S	**F**	**F**	**F**	S	S	S
PMU D	P	S	S	S	S	S	S	S	S	S	S	**F**	S	S	**F**	**F**	**F**	**F**	**F**
	M	S	S	S	S	S	S	S	S	S	**F**	**F**	S	**F**	**F**	**F**	S	**F**	**F**
PMU E	P	S	S	S	S	S	S	S	S	S	S	**F**	S	S	**F**	**F**	**F**	S	**F**
	M	S	S	S	S	S	S	**F**	S	**F**	**F**	**F**	S	S	**F**	**F**	S	S	**F**
PMU F	P	S	S	S	S	S	S	**F**	S	S	S	**F**	S	**F**	**F**	**F**	S	S	S
	M	S	S	S	S	S	S	**F**	S	S	**F**	**F**	S	**F**	**F**	**F**	S	S	S
PMU G	P	S	S	S	S	S	S	S	S	S	S	**F**	S	S	**F**	**F**	**F**	S	**F**
	M	S	S	S	S	S	S	S	S	S	S	**F**	S	S	**F**	**F**	S	S	**F**
PMU H	P	S	**F**	S	S	**F**	S	S	**F**	S	S	S	S	S	**F**	**F**	S	S	S
	M	S	**F**	S	S	**F**	S	S	**F**	S	S	S	S	S	**F**	**F**	S	S	S

TVE: total vector error; FE: frequency error; RFE: rate of change of frequency error; RT: response time; DT: delay time; MO: maximum over/under shoot.

TABLE VI
INTEROPERABILITY TEST RESULT SUMMARY

Device		Clock A				Clock B				Clock C				Clock D			
		C1	C2	C3	C4	C1	C2	C3	C4	C1	C2	C3	C4	C1	C2	C3	C4
PMU A-1	P	S	S	**F**	**F**	N	N	N	N	**F**	**F**	**F**	**F**	S	S	**F**	**F**
	M	S	S	**F**	**F**					**F**	**F**	**F**	**F**	S	S	**F**	**F**
PMU B	P	N	N	N	N	S	S	**F**	**F**	N	N	N	N	N	N	N	N
	M					S	S	**F**	**F**								
PMU C	P	S	S	**F**	**F**	N	N	N	N	S	S	**F**	**F**	S	S	**F**	**F**
	M	S	S	S	**F**					S	S	**F**	**F**	S	S	S	**F**
PMU F	P	S	**F**	**F**	**F**	N	N	N	N	S	**F**	**F**	**F**	S	**F**	**F**	**F**
	M	S	**F**	**F**	**F**					S	**F**	**F**	**F**	S	**F**	**F**	**F**

TABLE VII
TEST RESULTS FOR APPLICATION TEST USING VARIOUS PMUS

PMU at End S	PMU at End R		
	PMU A-1	PMU C	PMU F
	Estimated Location Error (%)	Estimated Location Error (%)	Estimated Location Error (%)
PMU A-1	1.173	2.909	0.852
PMU C	1.454	1.448	1.449
PMU F	0.473	2.571	1.018

C. Application Performance

Three PMUs and PMU-enabled IEDs are selected to perform the application test. The reference GPS receiver is used to synchronize the PMUs at each end, sending end and receiving end, denoted as "S" and "R" respectively. The tests include the configuration of PMUs from the same vendor for both ends and the PMUs from different vendors at each end. The estimated locations and errors for the fault variations defined in Table III are summarized in Table VII. The location error is calculated as follows:

$$l_{Err} = \frac{|l_R - l_M|}{l_R} \times 100\% \quad (5)$$

where l_R and l_M stands for the reference value and measured value. For each pair of PMUs, the mean value of estimated location errors for continuous measurements in two seconds is recorded. Test results show that the fault location errors using different pairs of PMUs vary from 0.4% to 2.9%, which correspond to the configuration of PMU F at End S while PMU A-1 at End R, and PMU A-1 at End S while PMU C at End R respectively.

VI. CONCLUSIONS

A new test methodology for verifying the interoperability and application performance of PMUs and PMU-enabled IEDs at device and system level is proposed in the paper. Reference signal and test scenarios for two types of tests are described. A reference PMU model is developed and implemented in a newly developed synchrophasor test system. Nine PMUs from eight different vendors and four commercial GPS receivers providing various types of time synchronization options were used to perform interoperability and application tests. The conclusions are summarized as follows:

- Most PMUs satisfied the steady state performance requirement, but none of them meets conformance under all the dynamic conditions;
- The interoperability issues between PMUs and time synchronization options can be identified using the test method;
- The application test method used for fault location can be extended to other types of applications, such as state estimation and voltage stability.
- The feedbacks received from vendors from reviewing the test results were instructive due to complexity of setting up some IEDs.

VII. ACKNOWLEDGEMENTS

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