Verifying Interoperability and Application Performance of PDCs in Synchrophasor System Solution

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***Abstract*—This paper presents a new test methodology for verifying the conformance performance of core PDC functionalities, the interoperability and application performance of synchrophasor system solution containing PMUs, PDCs, and communication network. Two types of tests are defined to evaluate the performance of synchrophasors system components from two different aspects: design and application. The interoperability between PMUs and PDCs can be verified by a design test. A fault location algorithm using two-end synchronized measurement is used to evaluate the application performance. We have developed a special device, referred to as "Impairator." that can emulate different network conditions by introducing impairments such as packet losses and delays. In addition, the impairator can measure performance characteristics of PDCs, such as data processing time. Nine commercial PMUs, three PDCs, and reference GPS receiver are selected to perform the tests. The test results at the end show that the PDCs meet most of the functional requirements, and interoperability issues exist between the PMUs and PDCs of different vendors.**

***Index Terms:*—phasor measurement unit (PMU), phasor data concentrator (PDC), intelligent electronic device (IED), synchrophasor, electric power grid, fault location**

I. INTRODUCTION

Synchrophasors were first introduced almost 30 years ago and are still under research. This technology allows measurements in different locations to be synchronized and time-aligned, and then combined to provide a comprehensive view of an entire region or interconnection. Synchrophasors are usually provided by Phasor Measurement Units (PMUs). The PMUs enable system analysis to determine the dynamic behavior of the power system and to pinpoint the exact causes that may lead to a catastrophic failure of the power system. Several prior works discuss the new applications to perform power system monitoring, protection and control using synchrophasors [1]-[6].

As a result of the American Recovery and Reinvestment Act (ARRA) funding and projects coordinated by the Department of Energy, and other industry efforts, it is expected that the number of installed PMUs and PMU-enabled Intelligent Electronic Devices (IEDs) will grow dramatically in the next 5-10 years. This asset will require costly solutions for substation installation, communications, data integration, and visualization.

The risks of the asset becoming stranded are real and are caused by the integration approaches used in the synchronized sampling technology implementation today:

- Multi-vendor PMUs and PMU-enabled IEDs ;
- Various time synchronization options;
- Different PDC and communication network options.

The mitigation of the risk requires reliance on standards and appropriate testing to ensure application compliance and design conformance across multiple PMU types and synchrophasor system designs. The standard IEEE.C37.118-2005 defines synchrophasor measurements used in the power system applications [7]. The dynamic performance requirements are captured in IEEE C37.118.1-2011 [8]. The Performance and Standards Task Team (PSTT) of the North American Synchrophasor Initiative (NASPI) issued a PMU system testing and calibration guide [9]. The communication requirements for PMUs are defined in IEEE C37.118.2-2011 [10].

While many efforts have been focused on testing individual PMUs [11]-[17], the application performance assessment tests have not been addressed by previous studies. The interoperability tests for synchrophasor system solutions consisting of many diverse types of the PMUs, time synchronization methods, communication options and PDCs are difficult to define since the draft "Guide for Phasor Data Concentrator Requirements for Power System Protection, Control and Monitoring" [18] only gives the functional requirements, but not specific performance indices.

This paper is structured as follows. In Section II we discuss the methodologies and procedures for performing design and application tests for PDCs. In Section III we discuss the design of network testbed. In Section IV we discuss the synchrophasor lab testbed. In Section V we present the results of comprehensive test studies. Finally, we conclude in Section VI.

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II. PDC TEST CLASSIFICATION

The objective of this section is to define two categories of tests, namely design and application tests.

A. PDC Design Test

Design tests consist of both conformance test and interoperability test, aimed at verifying the conformance performance of core PDC functionalities and interoperability with PMUs and PMU-enabled IEDs designed using existing standards.

The conformance requirements of the PDC functions are defined in "Guide for Phasor Data Concentrator Requirement for Power System Protection, Control, and Monitoring" [18]. We verify the conformance requirement by calculating the PDC Data Processing Time, and checking whether the amplitudes, phase and Total Vector Error (TVE) in the PDC output data stream meet the requirements defined in C37.118-2005 [7] and C37.118.1 [8].

The draft of PDC standard [18] gives a summary description of eighteen functions a PDC can perform: (i) Data alignment; (ii) Data communication; (iii) Data validation; (iv) Synchrophasor data transfer protocol support; (v) Synchrophasor data transfer protocol conversion; (vi) Format and Coordinate Conversion; (vii) Latency calculation; (viii) Reporting rate conversion; (ix) Data Buffering; (x) Configuration; (xi)Phase and magnitude adjustment; (xii) PMU/PDC performance monitoring; (xiii) Phasor data gateway; (xiv) Data aggregation; (xv) Robustness; (xvi) Redundant data handling; (xvii) Duplicate data handling; (xviii) Data re-transmission request.

We primarily focus on verifying whether the PDCs under test have some/all of the functions mentioned above and whether they are working properly under test conditions.

In addition, one of the main PDC function performance indices, namely Data Processing Time (DPT), defined as the total processing time required for a PDC to receive, validate, re-sample, and time align all input data stream packets, and repack and send the data to an output port for one data record will be tested. Since the processing time can be randomly distributed, especially in case of software PDCs running on generic hardware platforms and operating systems, a statistical approach to measuring processing time shall be used. The above requirements for DPT correspond to the average processing time plus two times the value of the standard deviation.

In our tests, the communication network is also considered as an important interchangeable part in the test since it may be implemented using different communication protocols in different settings [18]. The interoperability between PMUs, PMU-enabled IEDs, PDCs and associated communication network will be verified by interchanging equivalent parts in the system solutions, as shown in Table I. The PDCs include both software (PC-based) and hardware (standalone) solutions. The performance is evaluated by comparing the measured numerical results against specification defined in standards or applications.

TABLE I. THE DESCRIPTION FOR INTEROPERABILITY VERIFICATION

PDC under test	PMU	Communication Network	Performance Index
Software PDCs Hardware PDCs	Reference PMU and PMUs, PMU-enabled IEDs from different vendors	TCP/IP, UDP/IP, UDP/IP multi-casting	Function status and compliance test
		IPv4 and/or IPv6	
		Data Protocols (IEEE C37.118-2005, IEEE 1344 etc.)	

B. Application Test

The application tests are aimed at verifying performance compliance of specific applications, for instance, fault location, state estimation, etc. This is done by interchanging different PMUs, time synchronization options, PDCs and communication networks solutions. A fault location algorithm using two-end synchronized measurements is selected to perform the application test [19].

Fig. 1 shows one-line diagram of an equivalent circuit when a fault occurs on a transmission line. From the equivalent circuit diagram, the following equation holds:

$$\dot{V}_S = xZ_L \cdot \dot{I}_S + \dot{V}_f \quad (1)$$

$$\dot{V}_R = (1-x)Z_L \cdot \dot{I}_R + \dot{V}_f \quad (2)$$

Here V_S is the sending-end voltage, V_R is the receiving-end voltage, I_S is the sending-end current, I_R is the receiving-end current, Z_L is the line impedance.

Subtracting (1) from (2) to eliminate $\dot{V}_f$, we obtain the equation for computing location x using two-terminal voltage and current measurements:

$$x = \frac{\dot{V}_S - \dot{V}_R + Z_L \cdot \dot{I}_R}{Z_L \cdot (\dot{I}_S + \dot{I}_R)} \quad (2)$$

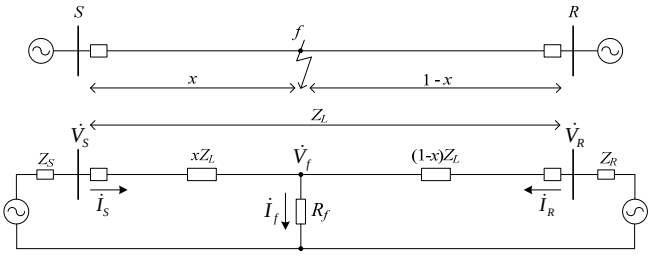

Figure 1. One-line diagram for a fault on transmission line

The above synchrophasor based fault location algorithm is selected to investigate how interchanging different PMUs and PMU-enabled IEDs, time synchronization methods, PDCs and communication conditions affect the application performances expressed as the relative error between the actual and estimated fault. The three elements of the system solution are tested individually. The tests results obtained when exchanging equivalent PMUs at two ends and different synchronization methods have been reported in [20].

The fault disturbances variations include different fault properties such as type, location, inception angle and fault resistance. We are also investigating the impact of delay and packet loss in the communication network on the final fault location results. Figure 2 shows an example how the packet loss may affect the fault location. To execute the fault location algorithm, we need to have the phasor measurements from both the sending and receiving end with the same timestamp. As long as one packet is lost, the algorithm would not be able to get the location at that specific point of time. We also assume that the circuit breaker will open shortly after the fault occurs. Therefore the number of synchoronphasor data we could receive and analyze is limited. Since we are taking the averaging result from multiple samples, the missing packet would degrade the accuracy of location determination result.

Figure 2. Impact of packet loss on two-terminal fault location algorithm

The test scenarios are summarized in Table II. We use transient voltages and currents generated from the ATP/EMTP system developed for testing [21]. The files recording voltage and current waveforms are read and fed to test system. The power network modeled in ATP is given in Figure 3.

TABLE II. TEST SCENARIOS FOR COMMUNICATION NETWORK TEST

Target	Test Configuration	Fault Variation
Communication Network: Latency: 0-500 ms Packet Loss: 5%-50%	Reference time clock	Location: 10%, 30%, 50%, 70%, 80% Type: SLG, LL, LLG,3L Inception: 0˚, 45˚, 90˚ Resistant: 0 Ω,25 Ω,50 Ω
	PMU and PMU-enabled IEDs: Reporting Rate: 30-60 samples/s	
	Software PDC Hardward PDC	

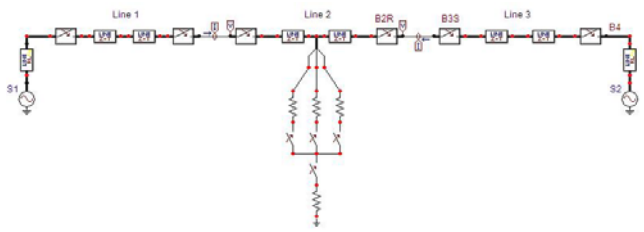

Figure 3. 230 kV power network in ATP model

III. COMMUNICATION NETWORK TESTBED DESIGN

The purpose of this testbed is to measure the impact of network impairments, such as delay and packet loss, on the performance of the power system applications like state estimation and fault location. We have considered a setting in which the PMUs and PDC utilize the protocol IEEE C37.118.2 for communication and control applications.

Figure 4 depicts a schematic view of the testbed. The testbed includes one or more PMUs and a PDC connected through a local area network (Ethernet). All packets exchanges between the PMUs and the PDC must traverse the network impairment generator, referred to as *impairator (described in Section III.A below)*, which provides the opportunity to emulate network conditions, such as packet loss and delay.

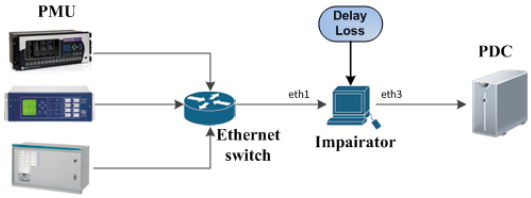

Figure 4. Evaluation testbed

A. *Impairator design and implementation*

The *impairator* was constructed using the Click modular router [22]. Click is an open source platform that enables fast prototyping of configurable routers. In Click, a router is decomposed into atomic design elements, referred to as *packet processing modules*. The modules have different functionality, such as packet forwarding, packet queuing, and packet classification. Click allows users to describe a router with all of its elements by using a simple configuration script. This architecture enables users to implement new router designs quickly and efficiently by 'clicking' several elements together to define their desired functionality.

The *impairator* acts as a 'bump-in-the-wire' network device. It is not observable through any network protocol – its solely purpose is to introduce certain impairments. The impairator has the ability to impart queuing delay (latency), and bit errors according to user defined scripts, such as:

```
FromDevice(eth1)->Queue->DelayUnqueue(T)->Queue->ToDevice(eth3)
FromDevice(eth3)->Queue->DelayUnqueue(T)->Queue->ToDevice(eth1)
```

Click script for PMU-PDC packet delay case

```
FromDevice(eth1)->RandomBitError(p)->ToDevice(eth3)
FromDevice(eth3)->RandomBitError(p)->ToDevice(eth1)
```

Click script for PMU-PDC packet loss case

Figure 5.A depicts the Click configuration used in this project. Both directions of packet transmission have a "forward with delay" element, which allows for controllable asymmetric packet delay. Figure 5.B depicts a Click configuration for imparting packet losses.

Since no packet loss elements are given in Click, the element Discard is implemented by introducing random bit errors. Bit errors in a packet will lead to checksum violations of the packet, which will lead to packet discard events resulting in packet loss. The bit error rate necessary to achieve the desired packet loss can be calculated by:

$$P(Loss_{rate}) = 1 - (1 - P(Bit_{Error_{Rate}}))^{Bit\_Size} \quad (4)$$

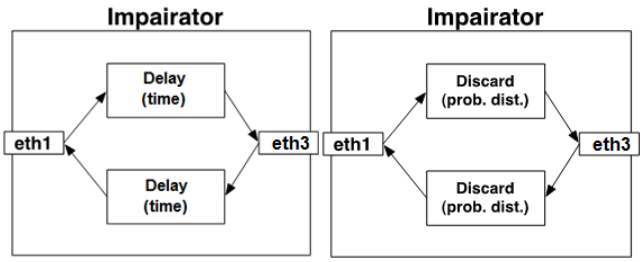

Figure 5. Impairator configuration for delay and packet losses

B. *PDC Data Processing Time (DPT) measurement*

The next objective was to measure PDC DPT defined in [18]. The base network configuration used in this test is equivalent to the packet loss and latency tests; however, an additional PDC was added to the environment. In this two-tier configuration, the first tier of PDCs provides an information aggregation function and forwards their summarized data to the top tier PDC. This experiment measures the processing time of the first tier PDC using the *impairator*. In this test the *impairator* was recording all ingress and egress packets for the PDC and using their internal identification parameters to calculate total data processing time. Figure 6 shows network configuration for data processing time management.

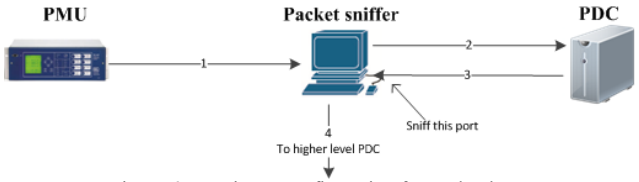

Figure 6. Impairator configuration for packet losses

To record the time of a packet's arrival and departure through the PDC, we use the open source Packet Capture library (PCAP) [23]. A capture of each packet both arriving and departing is recorded and then correlated to determine processing latency. PCAP captures packets and marks their arrival or departure times with microsecond granularity. Each packet capture's C37.118.2 header is examined and indexed in an arrival or departure data-structure using the ID header attribute. DPT is calculated for each departure packet by finding its corresponding arrival and comparing its recorded departure and arrival times.

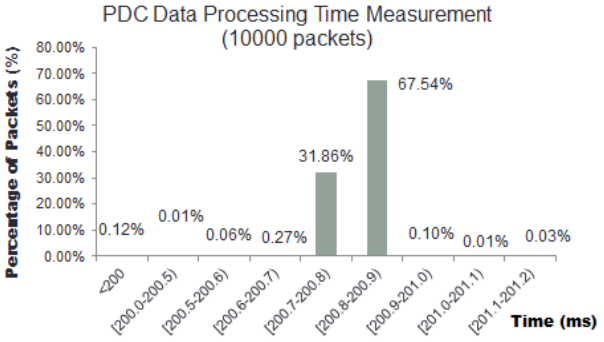

Figure 7. Test approach for design test

In the test, we record the DPT repeatedly for 10000 times and calculate the average processing time and its standard deviation. A typical PDC DPT distribution is shown below in Figure 7. The average DPT is 200.779ms, and the standard deviation is 1.060 ms.

IV. Test Implementation

The design and application tests are performed using a well-developed laboratory system for synchrophasor testing. It consists of a GPS receiver used to synchronize the system to UTC, a signal acquisition system used to generate and sample test signals up to 500 kHz, three voltage and current amplifiers connected to PMUs and PMU-enabled IEDs providing test signals at both typical and small voltage levels, three voltage attenuators and three current shunts. GPS signal, IRIG-B and IEEE 1588 v2 are available for various synchrophasor devices. Two software PDCs are installed in a Windows XP platform with Intel P4 2.4GHz CPU and 1GB of RAM. A series of software models is developed in LabVIEW [24][25].

Figure 7 shows the test approach for the design test, and Figure 8 shows the overall architecture for the application test.

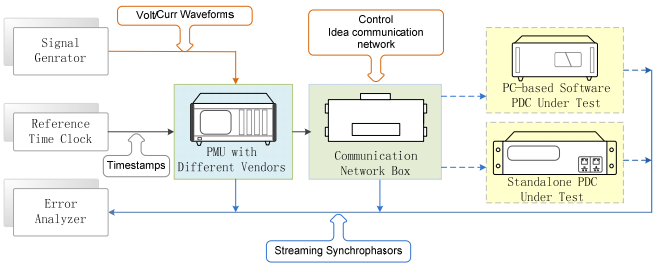

Figure 7. Test approach for design test

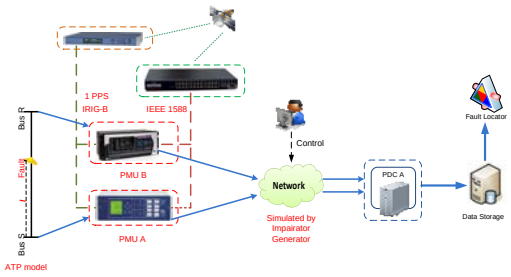

Figure 8. Applicatoin test overall architecture

V. Test Results

Preliminary test results from performing the conformance test, interoperability test and application test are presented in this section.

A. *Conformance Test*

Two software PDCs and a hardware PDC are selected to perform the conformance test, and they are denoted as A-C. The test results are summarized in Table III, in which "S" stands for "satisfied" while "F" stands for "failure", "N" stands for "No function". Per the reference functions defined in [18], some of PDCs did not have well-defined functions and therefore they are not tested.

TABLE III. PDC CONFORMANCE TEST RESULT

Functions under test	PDC A	PDC B	PDC C
Data Alignment	S	S	S
Data Communication	S	S	S
Data Validation	S	S	S
Synchrophasor data transfer protocol support	**IEEE C37.118**	**IEEE C37.118 Comtrade**	**IEEE C37.118**
Synchrophasor data transfer protocols conversion	S	S	S
Format and coordinate conversion	S	S	S
Latency calculation	S	S	S
Reporting rate conversion	S	S	S
Data Buffering	S	S	S
Configuration	S	S	S
Phase and magnitude adjustment	S	S	S
PMU/PDC Performance Monitoring	S	S	S
Data gateway	S	S	S
Data Aggregation	Not well-defined yet, not tested		
Robustness	Not well-defined yet, not tested		
Redundant data handling	S	S	S
Duplicate data handling	Not well-defined yet, not tested		
Data re-transmission request	N	N	N

B. *Interoperability Test*

Nine commercial PMUs and PMU-enabled IEDs, denoted as A-H, from eight different vendors were selected to perform the interoperability test between PMUs and PDCs. The test results are summarized in Table IV, in which "S" stands for "satisfied" while "F" stands for "failure".

PMU A-1 is an upgraded firmware of PMU A. It is noted that some PMUs are not interoperable with some PDCs. For instance, vendor claims that PDC B requires an additional adapter to support serial communication. And PDC C only supports serial port communication, but it has two Ethernet ports available for upgrade.

C. *Applicatoin Performance Test*

The reference GPS receiver is used to synchronize the PMUs at the sending end and receiving end, denoted as "S" and "R" respectively. The tests include the configurations of communication network gear generating different delay and packet losses. And the PMU's reporting rate will range from 0-500ms.

TABLE IV. PDCS AND PMUS INTEROPERABILITY TEST RESULT

PMU #	A	A-1	B	C	D	E	F	G	H
PDC A	S	S	S	S	S	S	S	S	S
PDC B	**F**	**F**	**F**	S	S	S	S	S	S
PDC C	S	S	S	**F**	**F**	**F**	**F**	**F**	**F**

1) *Impact of delays*

The tests show that the fault location algorithm is very tolerant to delays. As long as the PDC receives the packets from the PMUs and resends them to the application, the application will give correct results. However if the delay exceeds a certain threshold, the packets will be ignored by the PDC and therefore and applications will not function properly.

2) *Impact pakcet loss*

We assume that the circuit breaker will open 0.1s after the fault occurs. Hence the number of synchoronphasor data we could receive and analyze is limited. The test results (fault type: BC, location 10%) in Table V and Figure 9 shows that:

- Larger data loss will cause greater uncertainties (error deviation) impact on the final results.
- Larger data loss also dramatically increases the possibility of estimation failure.
- With increased PMU reporting rates, it could reduce the impact of data loss.

TABLE V. IMPACT OF DATA LOSS ON APPLICATION TEST

Bit Err Rate	Loss Rate	Dev.	Fail	Bit Err Rate	Loss Rate	Dev.	Fail
PMU reporting rate: 30samples/s				**PMU reporting rate: 60samples/s**			
0.001%	4.34%	1.567%	0.07%	0.001%	4.34%	1.097%	0.00%
0.003%	12.45%	2.713%	1.21%	0.003%	12.45%	2.038%	0.02%
0.005%	19.88%	3.963%	4.63%	0.005%	19.88%	2.905%	0.21%
0.008%	29.85%	4.660%	12.95%	0.008%	29.85%	3.896%	1.70%
0.010%	35.80%	4.965%	19.92%	0.010%	35.80%	4.265%	4.33%
0.012%	41.25%	5.242%	28.04%	0.012%	41.25%	4.734%	8.01%
0.015%	48.56%	5.492%	40.38%	0.015%	48.56%	4.826%	15.81%

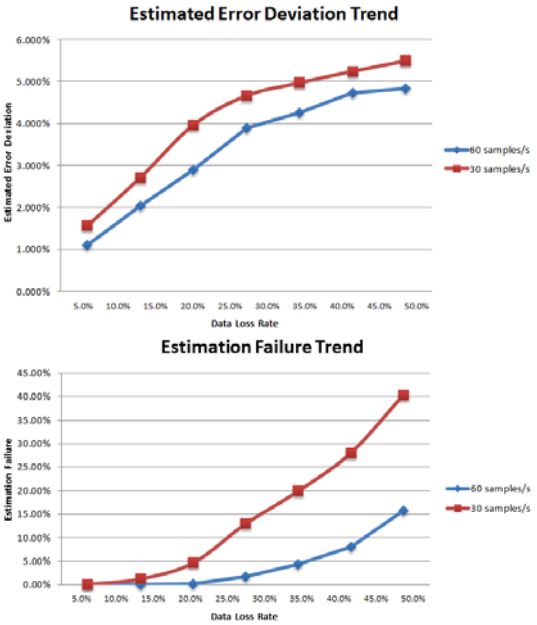

Figure 9. Impact of Data loss on Applicatoin Test

VI. CONCLUSIONS

We propose a new test methodology for verifying the conformance performance of core PDC functionalities, the interoperability and application performance of PDCs when connected to PMUs through a communication networks. A communication network toolbox called "Impairator" is developed and implemented in a newly implemented synchrophasor testbed. Nine PMUs and three PDCs with different communication network options were used to perform the design and application tests. The conclusions are summarized as follows:

- Design tests consist of both conformance test and interoperability test. In the conformance test, PDCs meet most of the functional requirements in [18]. However, since this guide is still under draft, further efforts are needed to check conformance of newly developed functional requirements and compliance of application performance requirements.
- The interoperability tests show that the interoperability issues between PMUs and PDCs exist as different PMUs use different communication methods, some use serial port communication only, some use Ethernet communication only while a few support both. At the same time, some PDCs do not support serial port communication while the others only support serial port communication. But this problem may be solved by upgrading or adding additional equipment.
- The communication network toolbox "Impairator" is able to measure the PDC's data processing time, and generate impairment used in application test. The test results show that the final location will have larger errors and uncertainties as the packet loss grows in the communication network. However this impact may be alleviated by increasing the PMUs' reporting rate. This method can be further extended to other types of applications, such as state estimation and voltage stability.

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