APPLICATION OF DIGITAL SIMULATORS IN TESTING DISTANCE RELAYS

C.W. Fromen, D.R. Sevcik
Houston Light & Power Company

M. Kezunovic, Y.Q. Xia, Y. Guo
Texas A&M University

M. Hammam
Electric Power Research Institute

U. S. A.

Abstract: Experience of digital simulator application in testing distance relays is discussed in this paper. The main application issues are as follows: automated testing of distance relay operating characteristics; synchronized testing of two-terminal relaying schemes; modeling and simulation of power swings; automated batch execution of a large number of transient tests; compliance requirements for power amplifiers.

Keywords: *Digital Power System Simulator, Protective Relay Testing, Distance Relay, Relay Operating Characteristic, Transient Modeling and Simulation*

1. INTRODUCTION

Recent developments of digital simulators for protective relay testing offer performance characteristics and user flexibility not matched by any of the previously known testing equipment [1-7]. Availability of the simulators gives new experiences from testing protective relays using the new capabilities.

This paper reports on recent digital simulator evaluation activities undertaken by Texas A&M University with sponsorship of EPRI and participation from Houston Lighting and Power (HL&P) Company and Western Area Power Administration (WAPA). The simulator being evaluated is designed for EPRI and member utilities. Some initial experiences using distance relays have been reported in a recent IEEE paper [8]. Further analysis of the digital simulator applications reported in this paper includes the following issues: automated testing of distance relay operating characteristics; synchronized testing of two-terminal relaying schemes; modeling and simulation of power swings; automated batch execution of a large number of transient tests; compliance requirements for power amplifiers.

This paper has been presented at the First International Conference on Digital Power System Simulators - ICDS '95, College Station, Texas, U.S.A., April 5-7, 1995.

2. TESTING OF OPERATING CHARACTERISTIC

This testing application was selected to evaluate simulator performance when used for characterization of the relay operating characteristics.

2.1 One Terminal System Representation

A one-terminal system representation model as shown in Fig.1 is used to obtain test waveforms. In the figure, Z_S is the equivalent source impedance, E is the phase-A source voltage which drives the fault current, I_L is the phase-A load current. We use Z_f to represent the fault impedance which includes the line impedance from the relaying point to the fault and the fault impedance combined with the in-feed effect. To obtain a complete characteristic, we assume that phase angle of Z_f changes from 0° to 360°. Using this model with different types of faults at F, we have derived the relaying voltages and currents for the single-line-to-ground (A-G), double-line-to-ground (BC-G), line-to-line (BC) and three-phase faults (ABC).

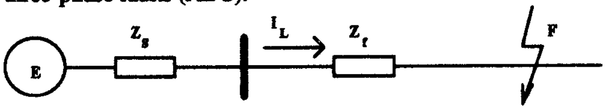
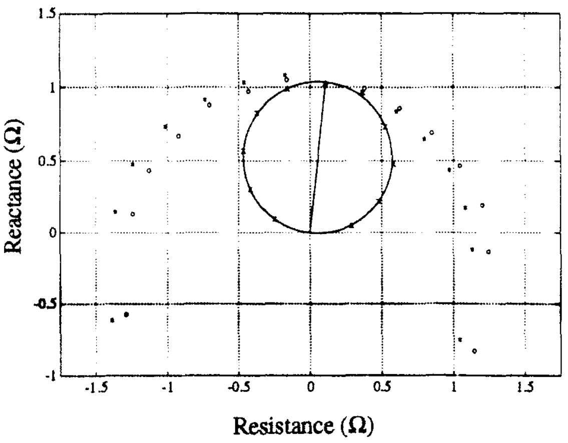


Fig.1 One terminal system representation model

For the relay under test, the input signals (three phase voltages and currents) contain at least two sets of different phasor quantities, namely, prefault and fault signals. Details about test wave forms, test procedures and test results have been discussed in [8]. Fig.2 shows typical test results for a distance relay. Three test cases were selected for each fault type according to the type of the prefault test wave form. In Fig.2, 'x' represents Case I (no prefault current and voltage) test results; 'o' represents Case II (no prefault current, with prefault voltage) test results; '*' represents Case III (with full load prefault voltage and current) test results. Extensive tests have been conducted including:

- different cases or prefault conditions
- different faults for the same relay
- different relays (five relays) for the same fault
- different load currents
- different source impedance ratio



x: Case I, o: Case II, *: Case III
Fig.2 Test results: ABC fault for Relay A using one-terminal system representation

Five different distance relays have been tested for different fault types and cases. The results reveal that this test method can be used to verify design features of phasor operating characteristic [8].

The test methodology using one-terminal representation model is efficient to verify design of phasor operating characteristics under different prefault conditions. It can also be used to evaluate application performance.

2.2 Two Terminal System Representation

The one-terminal representation model is used to test the phasor operating characteristic by changing the angle of Z_f from 0° to 360°. It is very efficient in verifying design of the operating characteristic. Impedance Z_f represents the line equivalent impedance from the relaying point to the fault containing the fault resistance and the far-end in-feed effect.

The tripping boundary in the first quadrant is most important for a relay under service. An exception may be the case when distance relays are used for series capacitor compensated lines. The tripping boundary in the fourth quadrant may also be meaningful. To test relay behavior for the far-end in-feed, a two-terminal phasor test model is used. The prefault and fault signals for the two ends, the sending end and the receiving end, have been derived by using a symmetrical component fault analysis method based on a two-terminal model as shown in Fig.3.

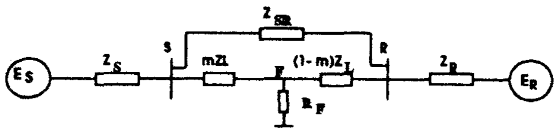
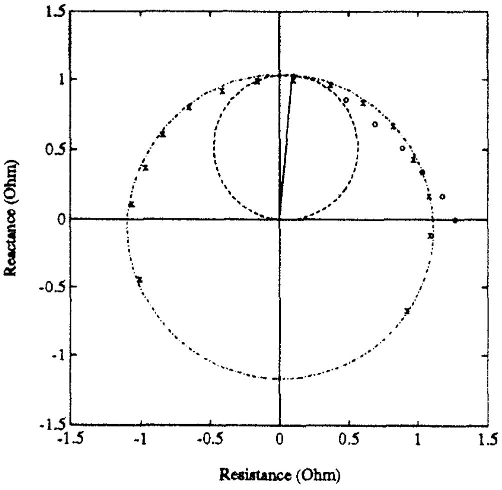


Fig.3 Two-terminal system representation model

In order to test operating characteristics of a distance relay taking into account the far-end in-feed effect, test waveforms (the three phase voltages and the three line currents) have been derived for a specified terminal based on the two-terminal representation model as shown in Fig.3. The relays have been tested for different faults using different waveforms. Fig.4 shows a typical set of test results for Relay B, single-line-to-ground fault.



'------': Theoretical steady-state characteristic
'-.-.-.-': Theoretical dynamic characteristic
'x': Test results using one-terminal model
'o': Test results using two-terminal model
Fig.4 Characteristic comparison of different model

It can be seen from the figure that the test results obtained by using the one-terminal model are very close to the theoretical characteristic. The results obtained by using the two-terminal model are different because of the far-end in-feed. The far-end in-feed effect depends on the fault resistance, the source impedance and the fault location.

3. TWO-TERMINAL BACK-TO-BACK TEST

This evaluation scenario was selected to demonstrate capability of digital simulators when used for back-to-back testing of two terminal relaying schemes for transmission lines.

3.1 Test strategy

Test set up for two-terminal testing is shown in Fig.5. A pair of distance relays are tested together with a certain relaying scheme. A time-delay device is used to simulate the communication channel between the two ends. The test signals for the two ends are generated synchronously and sent to the simulator terminals at the two ends.

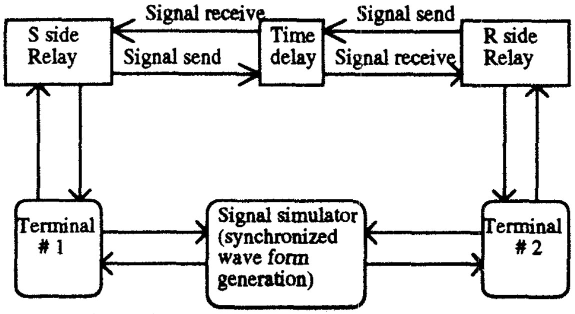


Fig.5 Two-terminal phasor testing strategy

3.2 Test Procedure

The two-terminal line model, as shown in Fig.3, is derived from a short line section in the HL&P system. The relays under test were set according to a specified relaying scheme. The test procedure is controlled by a computer program. For a given fault type, fault location and fault resistance, the test waveforms for both sides are generated from a set of equations that have been derived based on symmetrical component analysis. The test waveforms are sent out from the simulators to the relays under test, and the relay trip contacts are fed back. The operating times of the trip contact and the pilot signals of the two sides are saved in the computer memory before the next set of test waveforms are sent out to the relays. A test result summary file is automatically generated and saved on the disk after all the test are completed.

3.3 Test Results

Different relays have been tested with different relaying schemes for various faults including single-line-to-ground, line-to-line and three-phase faults. The relay schemes include:

- basic step distance (no pilot)
- permissive underreach transfer trip
- permissive overreach transfer trip
- blocking

Internal faults along the line from the local busbar to the far-end busbar as well as external faults behind the relaying points with different fault resistance have been simulated. A typical set of test results for Relay C is shown in Table I. The relay was set for permissive overreach transfer trip relaying scheme. Three-phase faults are located along the line, 10%, 20%, ..., 100% with different fault resistance 0, 0.25, 0.50 and 0.75Ω. In the table, the first column contains the values of fault resistance R_F; the second column contains the values of the line length m, from the relaying point to the fault. The third and the fourth columns contain the local relay operating time (TT#1) and the local relay signal-sending time (SST#1) respectively. The fifth and the sixth columns are the remote relay operating time (TT#2) and signal-sending time (SST#2).

Table I Three-phase fault test result for Relay C with permissive overreach scheme

R_F	M	TT#1	SST#1	TT#2	SST#2
0.00	0.10	14.42	14.39	23.94	12.74
0.00	0.20	15.17	12.49	14.32	14.12
0.00	0.30	12.94	12.79	13.14	12.94
0.00	0.40	13.84	13.82	14.09	13.47
0.00	0.50	14.77	14.52	14.14	14.02
0.00	0.60	13.17	13.19	13.44	13.02
0.00	**0.70**	**14.27**	**14.02**	**13.34**	**13.22**
0.00	0.80	13.77	13.72	13.34	12.92
0.00	0.90	25.61	14.39	13.37	15.19
0.00	1.00	24.14	12.92	13.99	13.87
0.25	0.10	15.92	15.77	24.84	17.59
0.25	0.20	16.47	16.39	25.29	18.02
0.25	0.30	16.69	16.37	25.91	16.34
0.25	0.40	16.79	16.67	25.74	16.59
0.25	0.50	19.49	16.82	18.27	15.67
0.25	0.60	19.64	16.99	18.22	15.42
0.25	0.70	23.79	16.92	15.57	15.27
0.25	0.80	26.04	17.07	17.79	17.29
0.25	0.90	25.66	18.82	17.39	17.07
0.25	1.00	25.86	18.89	17.02	16.57
0.50	0.10	xxxx	22.09	xxxx	xxxx
0.50	0.20	xxxx	16.92	xxxx	xxxx
0.50	0.30	xxxx	21.41	xxxx	xxxx
0.50	0.40	xxxx	15.79	xxxx	xxxx
0.50	0.50	33.96	20.59	30.04	24.86
0.50	0.60	28.66	15.42	25.09	20.16
0.50	0.70	xxxx	14.34	23.04	16.04
0.50	0.80	xxxx	xxxx	xxxx	21.11
0.50	0.90	xxxx	xxxx	xxxx	xxxx
0.50	1.00	xxxx	xxxx	15.69	15.49
0.75	0.10	xxxx	xxxx	xxxx	xxxx
0.75	0.20	xxxx	xxxx	xxxx	xxxx
0.75	0.30	xxxx	xxxx	xxxx	xxxx
0.75	0.40	xxxx	xxxx	xxxx	xxxx
0.75	0.50	xxxx	xxxx	xxxx	xxxx
0.75	0.60	xxxx	xxxx	xxxx	xxxx
0.75	0.70	xxxx	xxxx	xxxx	xxxx
0.75	0.80	xxxx	xxxx	xxxx	16.09
0.75	0.90	xxxx	xxxx	xxxx	xxxx
0.75	1.00	xxxx	xxxx	xxxx	xxxx

It can be seen from the test results that the two relays with pilot signal channel can protect the whole line if the fault resistance is smaller than 0.25Ω. The relays can not cover the whole line if the fault resistance is larger than 0.50Ω. If the fault resistance is larger than 0.75Ω, the relays can not respond to three-phase faults at any point of the line. The test results also show that different relaying schemes have different fault resistance coverage. Relay designs with different polarization schemes also affect the fault resistance coverage ability.

4. SIMULATION OF POWER SWINGS

Simulation of power swings is an important capability of the digital simulator design. The use of this feature in the digital simulator is illustrated in this section.

4.1 Modeling of Power Swings

A two-terminal model shown in Fig.6 is used to derive the swing test signals. The system parameters are based on the HL&P system.

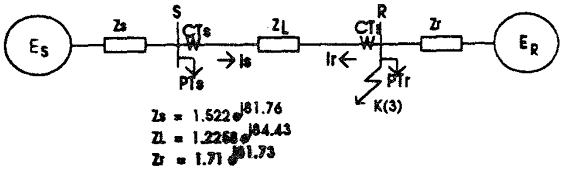


Fig.6 Two-terminal model for power swing study

Suppose a fault occurs outside the line at the R busbar as shown in Fig.6. The fault is cleared after 5 cycles. This disturbance may cause power swing after the fault is cleared. A swing period of 100 cycles is simulated. The frequency at the receiving end (R side) is fixed at a constant value f_0. The frequency of the sending end (S side) is expressed according to three periods, prefault (3 cycles), fault (5 cycles) and postfault (100 cycles) periods, as follows:

$$f=\begin{cases} f_0 & 0\le t\le t_1 \\ f_0 & t_1\le t\le t_2 \\ f_0+f_k(t-t_2) & t_2\le t\le t_3 \end{cases}$$

Test waveforms have been derived mathematically. Different swing frequency deviation from the fundamental frequency (60Hz) have been used to test the distance relays.

4.2 Testing of the Power Swing Block Function

Under power swing condition, the impedance locus may enter an operating zone to cause an impedance measuring unit to issue a trip signal. Usually, a power swing block unit is used to block the relay operation under swing condition. An inner and outer zone boundaries and timer constitute a swing block unit. If the impedance locus enters the inner zone boundary from the outer zone boundary, and the time is longer than a set value, then the unit will block the relay trip.

The two terminal equivalent model is reduced from a section in HL&P system. The equivalent source impedance at R side is little bit higher than that at S side. Suppose the system swing exists on the line, the impedance locus will enter the operating zones of the relays at both S and R sides.

Relay C is used as an example to illustrate the power swing block unit as shown in Fig.7. The inner zone boundary is formed by the A-B zone 3 or zone 2 phase fault characteristic. An additional power swing block starting characteristic, zone 6, is set concentric with the zone 3 or zone 2 characteristic depending on the zone 3 direction. If the power system A-B phase impedance locus enters the operating area of the starting characteristic, which has an adjustable timer setting Ts of 20-90 ms, and takes longer than this value to enter the fault characteristic, $|T_0-T_i|>$Ts, the power swing blocking unit will block the selected zones if the A-B phase impedance does eventually pass into the fault characteristic area.

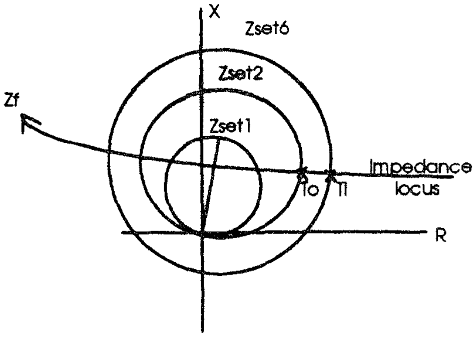


Fig.7 A typical power swing block scheme

4.3 Test Results

Different swing frequency increase rates have been simulated. Table II and III list the times it takes the locus to travel from the starting boundary to the other boundary. The times are measured by the relays at the two sides.

Table II Times (ms) measured from the starting to the other boundary (Ratio of change of swing frequency = 1.0Hz/s)

S side $\lvert T_i-T_o\rvert$	R side $\lvert T_i-T_o\rvert$
50.7 (Z6→Z2)	57.6 (Z6→Z2)
39.8 (Z2→Z6)	42.2 (Z2→Z6)
24.9 (Z6→Z2)	27.4 (Z6→Z2)
23.8 (Z2→Z6)	25.0 (Z2→Z6)
17.4 (Z6→Z2)	21.0 (Z6→Z2)

Table III Times (ms) measured from the starting to the other boundary (Ratio of change of swing frequency = 1.5Hz/s)

S side $\lvert T_i-T_o\rvert$	R side $\lvert T_i-T_o\rvert$
46.5(Z6→Z2)	47.6(Z6→Z2)
26.9(Z2→Z6)	37.0(Z2→Z6)
22.7(Z6→Z2)	21.4(Z6→Z2)
21.9(Z2→Z6)	19.3(Z2→Z6)
14.6(Z6→Z2)	16.8(Z6→Z2)
10.8(Z2→Z6)	16.1(Z2→Z6)
14.4(Z6→Z2)	14.9(Z6→Z2)
9.7(Z2→Z6)	14.8(Z2→Z6)

Different distance relays with different relay setting, the swing block unit disabled or enabled, have been tested using the generated waveforms. The relays were tested using two-terminal configuration. It can be seen from the test results that if the swing block unit is disabled or the swing frequency is higher than the value that causes the impedance locus passing time to be equal to the set value Ts, the relay will trip. Using simulators to simulate power swing condition and to test distance relay is useful to check the swing block unit and to select the set value.

5. AUTOMATIC TRANSIENT TESTING

Automatic transient testing of distance relays is an important feature that has been demonstrated using the digital simulator. This section summaries the test results.

A transmission line with its external system has been modeled using EMTP software. A short line (NBelt-King) and its external equivalents are modeled based on system configuration database and power flow data of Houston Power & Lighting Company. One-line reduced model of the line section is shown in Fig.8.

Case-by-case test is important for result analysis corresponding to test waveform. It is also very useful to verify the model of the actual system and relay settings. The most important requirement for simulator application in relay testing is large number of test cases. Different fault type, location, inception angle and fault impedance combinations result in a larger number of different cases. Batch file function has been developed to automatically generate test waveform using EMTP, to convert data into required format and to execute tests.

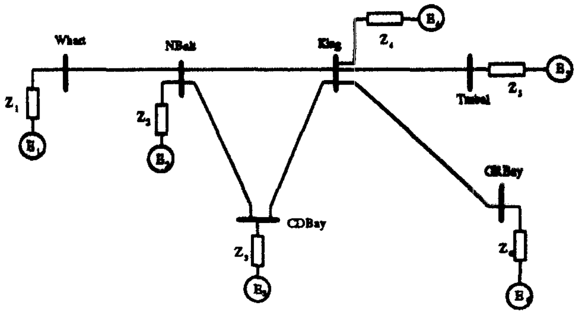
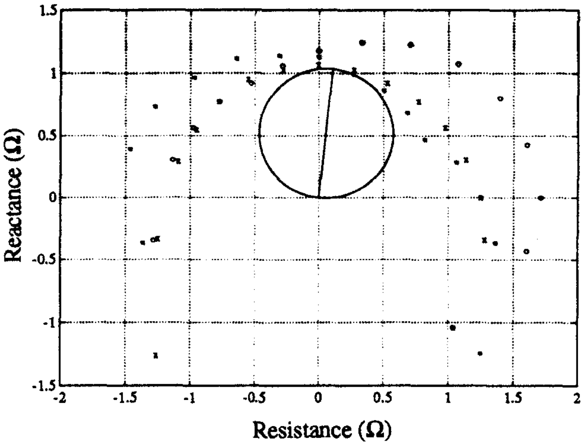


Fig.8 NBelt-King line reduced section

6. REQUIREMENTS FOR POWER AMPLIFIERS

Requirement for power amplifiers is dependent on technology/hardware implementation of the relay under test. Usually, low power amplifiers can meet requirement for testing static and microprocessor based relays. Electromechanical relays, however, need amplifiers with much higher power for both voltage and current channels.

When low power amplifiers are used to test an electromechanical relay, problems may be encountered. Here is an example that was encountered during an application in distance relay testing. When low power voltage amplifiers (maximum current output 400mA peak) were used to test phasor operating characteristic, the test results were not as expected. Fig.9 shows the test results.



x : AB fault ; o : BC fault ; * : CA fault

Fig.9 Test results using low power voltage amplifiers

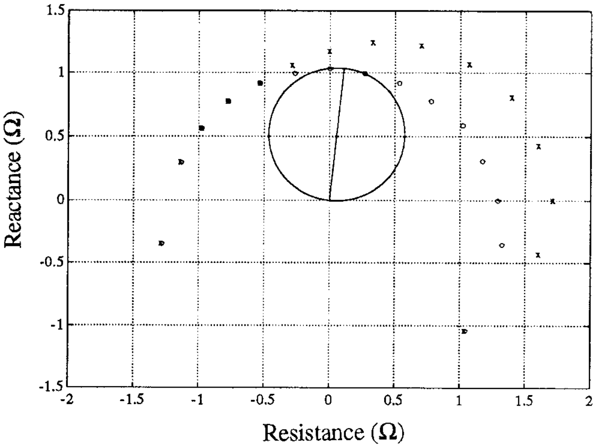
In an electromechanical distance relay, the voltage and current coils are coupled together. When a current in the current coil is high, the induced voltage at the voltage coil can drive a high current in the voltage amplifier circuit. The voltage amplifier was originally designed to have maximum capacity of 400mA (peak). The voltage amplifier may give up the control of the output, if the current is higher than the limited value. The voltage amplifiers can not control the outputs when the voltages at the relay terminals go high, which will drive high currents in the amplifier circuit.

Voltage amplifiers of high current have been used to repeat the tests. Comparison of the results obtained by using different voltage amplifiers are shown in Fig.10. It is obvious that the 'overreach' for BC faults is caused by the low current voltage amplifiers.

7. CONCLUSIONS

The evaluation report presented in this paper reveals the following features of the digital simulator:

- testing of phasor operating characteristics
- two terminal back-to-back testing
- power swing testing
- automatic transient testing
- power requirements for voltage amplifiers.



x : weak amplifier ; o : high power amplifier

Fig.10 Results by using different voltage amplifiers

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Charles W. Fromen received his B.Sc. degree in Electrical Engineering from Texas A&M University in 1968. He joined Houston Lighting & Power Company upon graduation. Since 1984, he has held the title of Senior Consulting Engineer. Mr. Fromen has been the HL&P Company representative to the IEEE Power Systems Relaying Committee since 1973 and is a member of that committee. He is a registered Professional Engineer in the State of Texas.

Donald R. Sevcik received his B.Sc. in Electrical Engineering from Texas A&M University in 1975. He was employed by Houston Lighting & Power Company in 1975 and is currently a Lead Engineer. He has worked in the following areas: Power Plant Electrical System (1975 to 1977), System Studies (1977 to 1979), and Transmission and Generation Protection (1979 to present). He is a registered Professional Engineer in the State of Texas and an IEEE member.

Mladen Kezunovic received his Dipl. Ing. degree in electrical engineering in 1974, and the M.S. and Ph.D. degree from the University of Kansas, in electrical engineering in 1977 and 1980 respectively. His industrial experience is with Westinghouse Electric Corporation in the U.S.A., and the Energoinvest Company in Sarajevo. His academic experience is with the University of Sarajevo and Washington State University. He has been with Texas A&M University since 1987 where he is an Associate Professor. He is member of the IEEE PSRC, member of CIGRE and a registered Professional Engineer in the State of Texas. Dr. Kezunovic is the chairman of the PSRC working group F-8 on " Digital Simulator Performance Requirements".

Yanquan Xia received his B.Sc. and M.Sc. degree from the Tianjin University, P. R. China, the Ph.D. degree from the Hong Kong Polytechnic, Hong Kong, all in Electrical Engineering in 1986, 1989 and 1993 respectively. He is currently a Post Doctorate Research Associate at Texas A&M University since 1993. He has several year industrial and academic experience, and authored and co-authored a number of IEEE and IEE papers. He is an IEEE member.

Yong Guo received his B.Sc. and M.Sc. degree from the Huazhong University of Science and Technology, China, all in Electrical Engineering in 1984 and 1987 respectively. He joined the same University as a Lecturer in 1987 and worked there until 1993. He is currently a Research Associate at Texas A&M University since 1993.

M. Hammam is a Project Manager at EPRI responsible for the Protective Relay Workstation Project. Ms. Hammam has been with EPRI since the Fall of 1993.