Impact of the Errors in the PMU Response on Synchrophasor-Based Fault Location Algorithms

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***Abstract*— Over the past decades, many synchrophasor applications have been developed but the performance under various PMU errors has not been explored and is unknown for most applications. This paper discusses the impact of PMU measurement errors and limitations originated from hardware implementation of various phasor estimation algorithms on the accuracy of the synchrophasor-based fault location application, in particular on the fault location algorithm that uses synchronized phasors at both line terminals. The application test procedure is implemented on a simple two-bus system modeled in ATP-EMTP with different types of fault scenarios simulated and various real PMUs exposed to the fault signals through hardware-in-the-loop testing. Results acquired from such evaluations provide invaluable knowledge about limitations and vulnerabilities of synchrophasor end-use applications.**

***Index Terms*—Application error; fault location; Phasor Measurement Unit; testing; hardware-in-the-loop; trustfulness.**

I. Introduction

The Phasor Measurement Unit (PMU), introduced in the 80s, is an instrument capable of measuring amplitude and phase angle of voltage and current phasors, as well as the frequency and rate of change of frequency. Phasor angle is defined as a relative displacement at a given location compared to the reference cosine signal at another location, both synchronized to the Coordinated Universal Time [1]. The synchronization is usually accomplished using the time reference signal from Global Positioning System of satellites [2]. Fast calculation and reporting of the PMU data helps capture and track high-resolution real-time information for new advanced applications and improves situational awareness of the grid states [3]-[8].

PMU measurements are employed in a large number of power system applications often implemented as Wide Area Monitoring, Protection and Control (WAMPAC) systems. PMU measurements are also applied in the model validation processes and are widely utilized in the system protection applications such as fault detection and location, out-of-step protection, oscillation detection, etc. [9]. To ensure the reliability and security of the infrastructure for synchrophasor-based end-use applications, good synchronization (better than 1 us), fast reliable communication network, and precise phase angle and magnitude measurements are needed [10].

Performance requirements of a PMU are specified in IEEE standards C37.118.1-2011 and C37.118.1a-2014 [11], [12]. Two classes of PMUs, namely the P and M performance class, are defined in the standards. The protection (P) class is focused more on the fast response rather than high precision. The opposite is required by the measurement (M) class PMUs. Each synchrophasor-capable Intelligent Electronic Device (IED) has to conform to at least one performance class. IEEE standard C37.118.1 specifies the type of the tests (i.e. steady state and dynamic state) and the maximum allowed measurements error, e.g., Total Vector Error (TVE), Frequency Error (FE) and Rate of Change of Frequency Error (ROF), which is defined for each reporting rate and performance class. The procedures and requirements for test equipment, e.g., timing reference, signal sources, calibration devices, and environmental conditions are specified in the IEEE Synchrophasor Measurement Test Suite Specification (TSS) report [13].

Significant research has been dedicated to compliance analysis of PMUs through calibration type-tests [14]-[20], and in-field test procedures [21]-[23]. The compliance with the standard requirements is confirmed by exposing PMUs to the input signals defined in the standard [24]. The laboratory test case studies through hardware-in-the-loop testing reveal noticeable inconsistencies among the phasor estimates obtained by PMUs from different manufacturers under the conditions not specified in the standards [25]-[28]. This is caused by different performance of various PMU estimation algorithms as well as physical hardware implementations. Further studies also demonstrated a difference between outcomes captured by PMUs in real-world and simulation results [29]. Such observations suggest that there is no guarantee that different end-use applications would perform satisfactorily even if the PMUs have passed all the standard type-test requirements. The impact of PMU errors is recognized as an important application issue. The North American SynchroPhasor Initiative has recently formed the PMU Application Requirements Task Force with a mission to define data quality requirements for each synchrophasor-based application, which is expected to speed up the deployment of the synchrophasor technology [30]. In this paper, the PMU response errors under the fault conditions are characterized and their impact on the performance of synchrophasor-based fault location algorithms that uses synchronized phasors at both line terminals is quantified.

The remainder of the paper is structured as follows. Section II briefly states the problem and elaborates on the selected fault location algorithm. Structure of the test setup as well as its functionality is highlighted in Section III. Experimental results and use case studies are presented in Section IV following by the concluding remarks in Section V.

II. Problem Statment

A. Synchrophasor-based Applications in Power Systems

One of the essential power system protection applications is certainly detection of the faults and locating where they are on transmission lines. The faults may be caused by a variety of reasons, e.g. failure of different equipment, severe weather conditions, human-induced accidents, animal interferences, etc. Timely detection and location of the faults in the network is of critical importance for maintaining the security and decreasing the risk of the loss of load and consequent financial losses. If efficiently employed, fast and time-synchronized PMU measurements can facilitate a more accurate fault detection and location in power systems. Considerable research has been devoted to developing fault detection and location algorithms using PMU measurements [31]-[42].

B. Synchropahsor-based Fault Location Algorithm

In this section details of one synchrophasor-based fault location algorithm that uses the synchronized data samples at both ends of the line are explained. This use case demonstrates how to evaluate the impact of PMU response errors under fault conditions on the fault location application outcome through hardware-in-the-loop testing.

This fault location technique uses symmetrical components, namely the negative, and positive sequence, of voltage and current waveforms as an input to the fault location algorithm. These values can be measured and reported by PMUs, or can be alternatively calculated from the reported voltage and current phasors. The equivalent negative and positive sequence network representations of the transmission line when fault occurs are demonstrated in Fig. 1 [3].

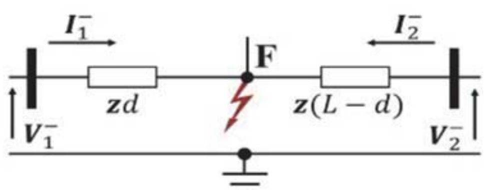

Fig. 1(a). Equivalent negative sequence network of the faulted TL.

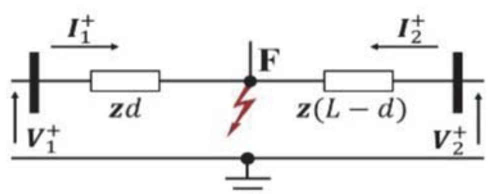

Fig. 1(b). Equivalent positive sequence network of the faulted TL.

From the equivalent circuits, the following equations can be derived:

$$\boldsymbol{V}_1^- - \boldsymbol{z}d\boldsymbol{I}_1^- - \boldsymbol{V}_2^- - \boldsymbol{z}(L-d)\boldsymbol{I}_2^- \quad (1)$$

$$\boldsymbol{V}_1^- - \boldsymbol{z}d\boldsymbol{I}_1^- - \boldsymbol{V}_2^- - \boldsymbol{z}(L-d)\boldsymbol{I}_2^- \quad (2)$$

Where the following nomenclature applies:

$\boldsymbol{z}$	Negative and positive sequence line impedance.
L	Total length of the transmission line.
d	Distance from the Bus 1 to the fault location.
$\boldsymbol{V}_{1,2}^-, \boldsymbol{V}_{1,2}^-$	Negative and positive sequence phase voltages at both ends of the line.
$\boldsymbol{I}_{1,2}^-, \boldsymbol{I}_{1,2}^-$	Negative and positive sequence phase currents at both line terminals.

Distance to the fault can be represented as a percentage of the line length L, as introduced in (3):

$$d\% - \frac{d}{L}100 \quad (3)$$

Combining equations (1) and (2), the following expression for the distance to the fault can be obtained:

$$d\% - 100\frac{(\boldsymbol{V}_1^- - \boldsymbol{V}_2^-)\boldsymbol{I}_2^- - (\boldsymbol{V}_1^- - \boldsymbol{V}_2^-)\boldsymbol{V}_2^-}{(\boldsymbol{V}_1^- - \boldsymbol{V}_2^-)(\boldsymbol{I}_1^- - \boldsymbol{I}_2^-) - (\boldsymbol{V}_1^- - \boldsymbol{V}_2^-)(\boldsymbol{I}_1^- - \boldsymbol{I}_2^-)} \quad (4)$$

III. Description of the Test Set-Up

The testbed platform used for characterizing the PMU response under fault conditions and evaluating the impact of the PMU errors on the fault location application outcome is implemented at Texas A&M University. The developed infrastructure is generic enough to be employed not only for quantifying the impact of PMU errors on fault location algorithms, but also performing studies on trustworthy assessment of any end-use power system application that uses PMU measurements. General structure of the test setup is depicted in Fig. 2. As shown in Fig. 2, the synchrophasor system consists of timing references, signal generator, power amplifiers, and data management and analytic tools. Timing reference provides GPS clock reference to the PMUs so that measurements from different devices are synchronized and time-stamped. Model of the network under evaluation is built in the ATP-EMTP software package environment. Various fault scenario use cases are simulated and waveforms are generated using the low voltage simulators. In order to have realistic measurements from the PMU, the applied signals must conform to the nominal level defined by the PMU device (i.e., normally 70 V_{rms} and 5 A_{rms} for voltage and current, respectively). Signals from the simulators are amplified to the nominal level using power amplifiers. Since the selected fault location algorithm requires measurements from both ends of the line, two PMU devices were fed simultaneously with the fault signals assuming they are located at both ends of the line. Each PMU is connected to the GPS antenna for the synchronization purposes and measured data streams from the devices are collected and fed to fault location algorithm for further evaluation purposes.

IV. Experimental Results

A. System Under Test

The network model under test, a 400kV, 100-mile long transmission line was built in the ATP-EMTP software environment. The selected fault location algorithm was evaluated under 30 different fault use case scenarios: the transmission line was exposed to various types of faults [i.e., single phase to ground (ag), phase to phase (ab), two phase to ground (abg), as well as three phase fault (abc)] and various possible locations along the line [e.g., 5%, 20% and 50% of the line length from the bus 1 terminal].

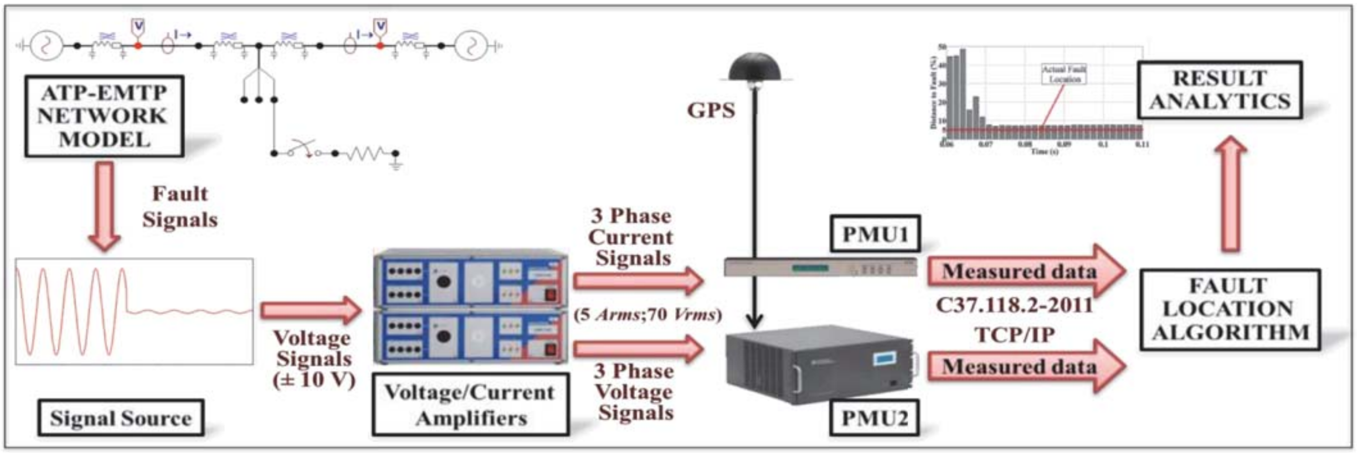

Fig. 2. Synchrophasor-based testbed set up for evaluation of the impact of PMU errors on the end-use applications.

Synchrophasor-based fault location algorithm sensitivity to the changes in the fault resistance was investigated as well. Three values of resistance were used in the simulations: 0, 20, and 100 ohms.

The schematic diagram of the simulated network with three different locations for the fault occurrence is depicted in Fig. 3(a)-(c). Fig 3(d)-(i) demonstrate simulated phase voltages at both ends of the line for the single line to ground (ag) fault with R_F=20 ohms fault resistance; Fig. 3 (d)-(f) illustrate the phase voltages at Bus 1 while the phase voltages at the Bus 2 are demonstrated in Fig. 3 (g)-(i). The waveform sampling frequency was set to 3.8 kHz. Parameters of the active networks L and R, as well as the transmission line characteristics are listed in Table I and Table II, respectively.

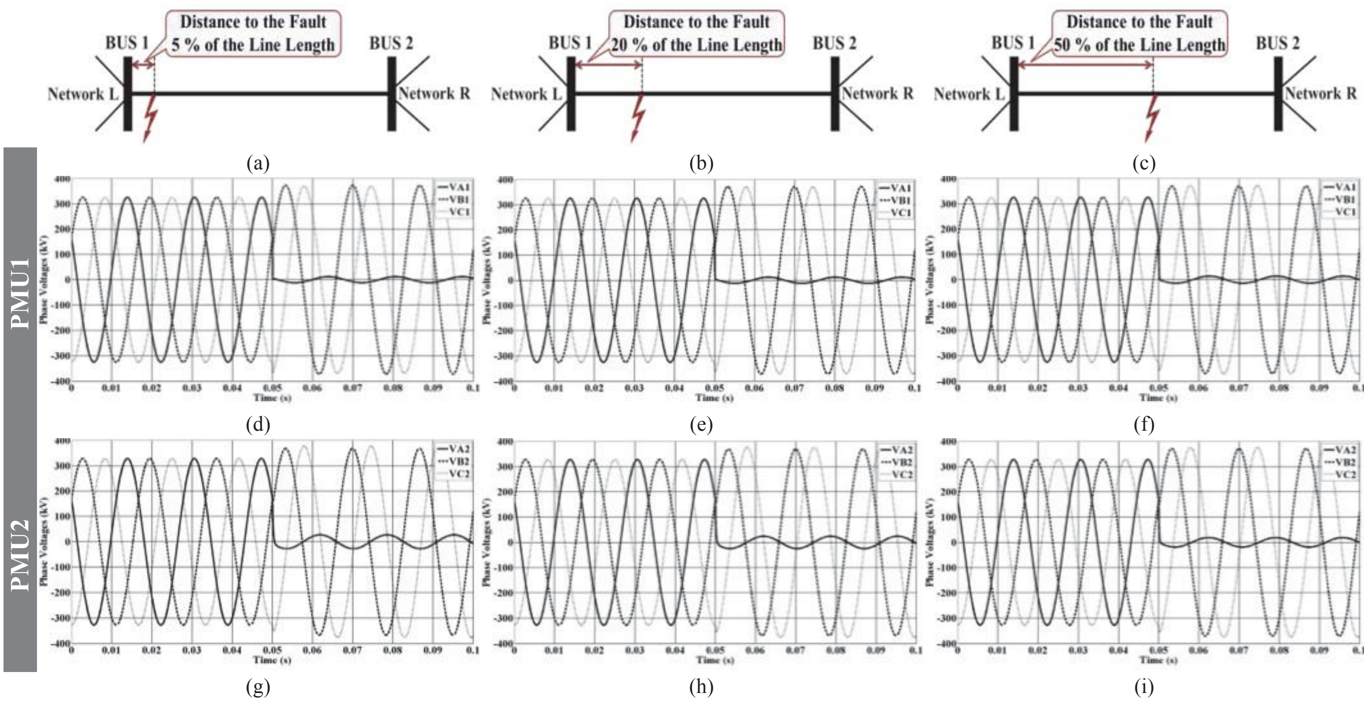

Fig. 3. Simulated phase voltages in the transmission line fault use case scenarios.

TABLE I. PARAMETERS OF THE ACTIVE NETWORKS

Parameters	*Network L*	*Network R*
V_{rms}^{LL} [V]	416000	400000
Frequency [Hz]	60	60
R^{zero}[Ω]	2.0371785	1.2732366
$R^{-,-}$[Ω]	1.0185892	0.6366183
L^{zero} [H]	0.10185892	0.0636618
$L^{-,-}$[H]	0.0509295	0.0318609

TABLE II. TRANSMISION LINE PARAMETERS

Parameters	*Resistance [Ω/km]*	*Inductance [mH/km]*
+ and - sequence	0.065	0.95493
Zero sequence	0.195	2.86479

B. Numerical Results and Discussions

Voltage and current waveforms simulated in the ATP-EMPT are scaled down to the level of ±5V and generated using the low voltage laboratory simulator. The low voltage signals are then amplified using the power amplifiers; since the simulator is only capable of generating the voltage signals, a voltage controlled current source was used for generating the corresponding three phase current signals. Two PMU devices were then exposed to the generated fault signals. Measurements from both devices are collected, merged, and stored in the database for further analysis. Sample PMU measurements acquired from both line terminals, during the single-line to ground fault (ag) for the three different location of the fault along the line (5%, 20% and 50% of the line length) are demonstrated in Fig. 4. Figures (a)-(c) and (d)-(f) illustrate the voltage phase magnitudes and corresponding phase angle measurements at Bus 1, respectively. Figures (g)-(l) demonstrate the PMU measurements at Bus 2, which actually highlights how this PMU responds under simulated fault conditions. As one can see from the sample results, after the fault occurs (t = 0.05s), there is a short period of time until the PMUs successfully detect the disturbance, which is mainly related to the delay of the signal generator response and another half a cycle period (i.e., 10ms) for the measurements to become reliable. PMU measurements are then submitted to the fault location algorithm and the results are depicted in Fig. 5.

Single line to ground fault was simulated with the three values of fault resistance: the bolted fault use case scenario (0 ohm) is illustrated in figures (a)-(c); the 20 ohm fault resistance use case scenario is depicted in figures 5(d)-(f); and the high-resistance 100 ohm fault scenario is illustrated in figures 5(g)-(k). From the results, it can be seen that during the higher resistance fault scenarios, the time taken to locate the fault is comparatively longer. Also it can be noticed that the minimum error is corresponding to the scenario when the fault has happened in the middle of the line, while it is at its highest when the fault occurs at the begging of the line. A summary of the results for all simulated fault scenarios is tabulated in Table III. All calculated errors corresponding to the studied fault location algorithm are within the 3% of the line length. It is worth mentioning that errors introduced by the communication network and phasor data concentrator have not been incorporated in this test case study while it is very important for such use case to be considered and be researched in future.

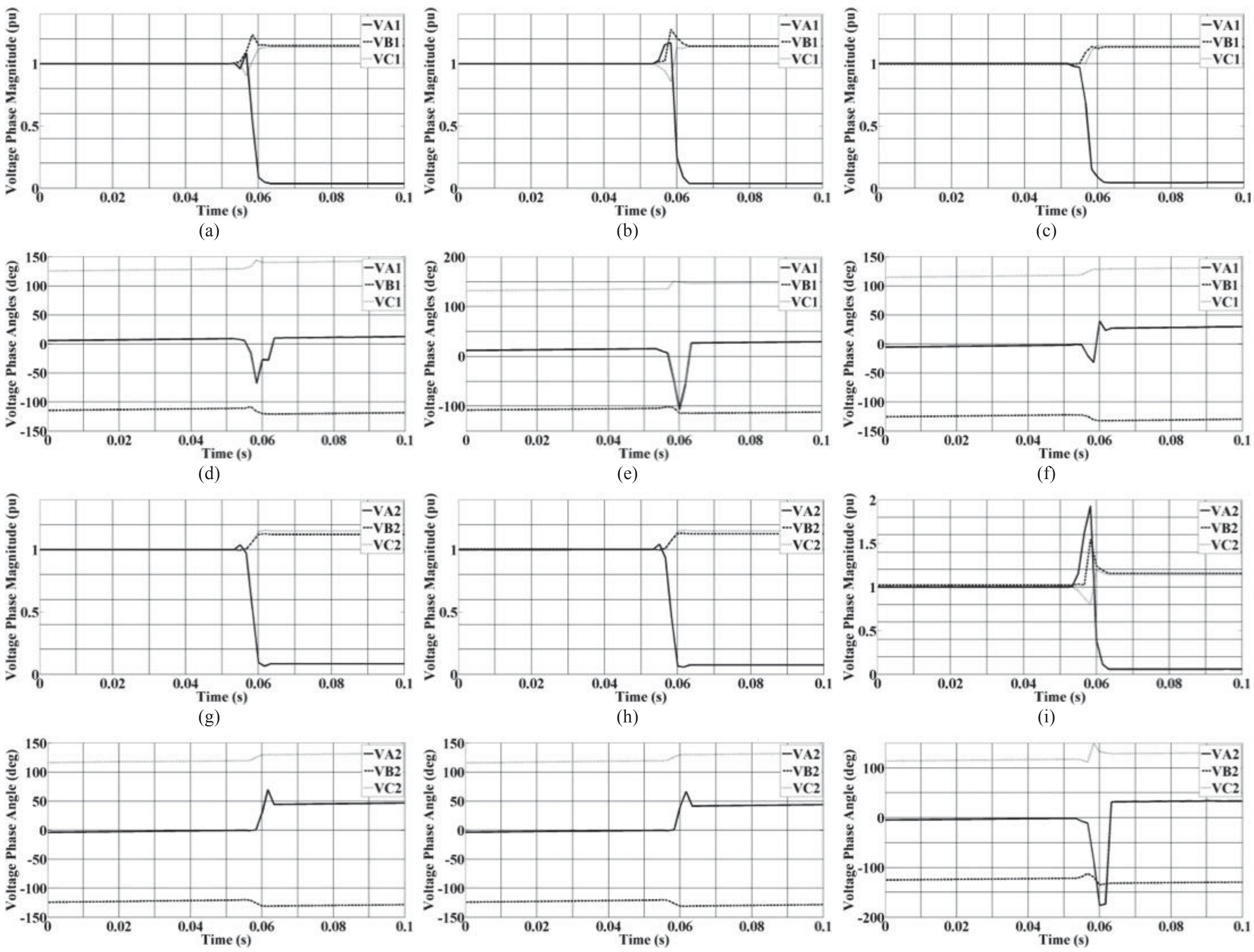

Fig. 4. PMU measurements: magnitudes and the phase angles at both ends of the faulted transmission line.

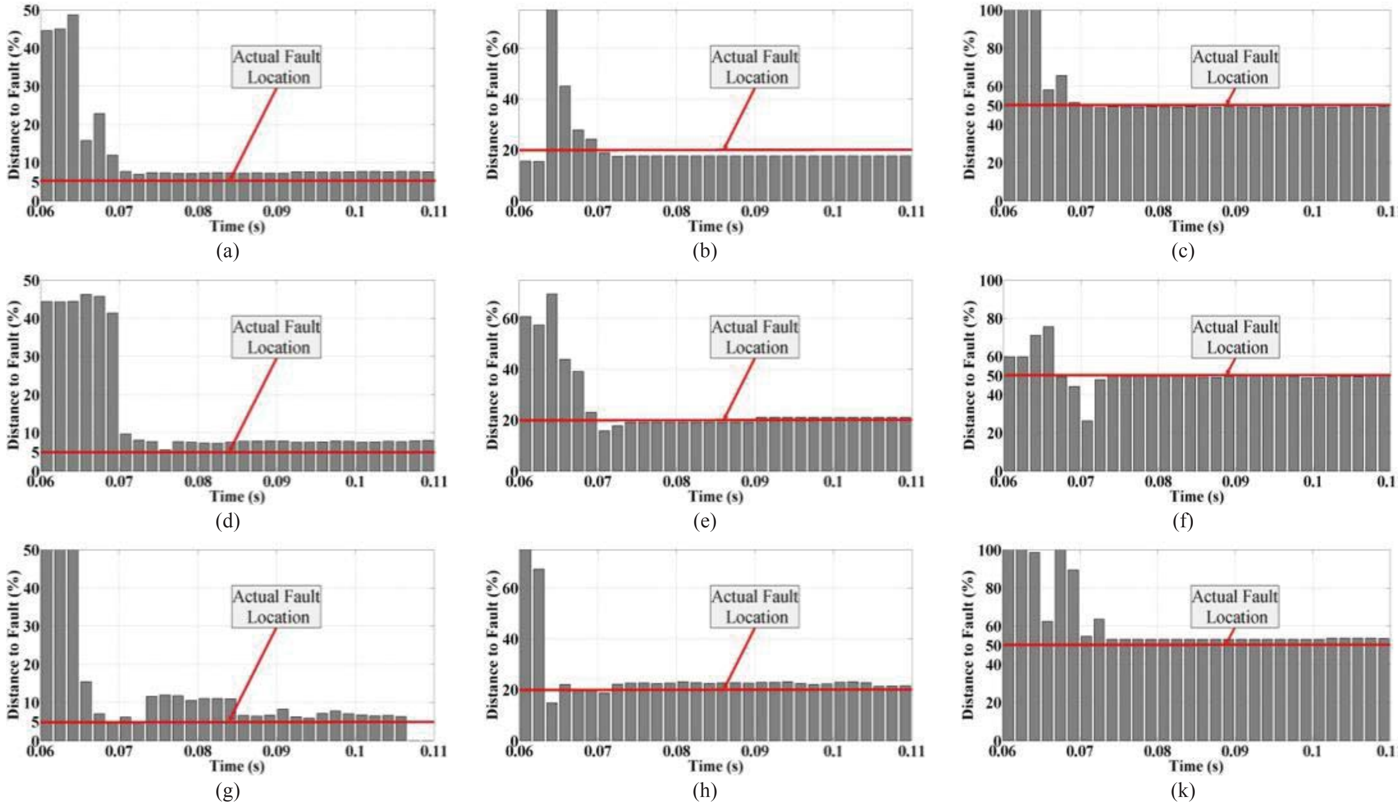

Fig. 5. Synchrophasor-based fault location algorithm performance: calculated fault locations for different fault use case scenarios.

V. Conclusions

The paper offers the following contributions:

- The PMU performance results obtained by using hardware-in-the-loop test facility to assess individual PMU response under the standard tests signals and different network prevailing conditions.
- A methodology on how to estimate the impact of PMU measurement errors under various scenarios on any synchrophasor-based end-use application.
- The impact of PMU errors on synchrophasor-based fault location algorithm requiring synchronized phasor measurements at both ends of a transmission line.
- The evidence of the importance of evaluating the impact of PMU errors on the end-use application and how the simulation results might be different with real–world measurements.

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TABLE III. Summary of the Fault Analisys

Fault Type	Fault Location (miles)	Fault Resistance (Ω)	Calculated Fault Location (miles)	Fault Location % Error
ag	5 (5%)	0	7.56	2.56%
	20 (20%)		18.24	1.76%
	50 (50%)		49.72	0.28%
	5 (5%)	20	8.6	3.6%
	20 (20%)		20.89	0.89%
	50 (50%)		49.84	0.16%
	5 (5%)	100	7.97	2.97%
	20 (20%)		22.16	2.16%
	50 (50%)		51.07	1.07%
abg	5 (5%)	0	6.93	1.93%
	20 (20%)		21.22	1.22%
	50 (50%)		50.78	0.78%
	5 (5%)	20	-	-
	20 (20%)		21.79	1.79%
	50 (50%)		48.32	1.68%
	5 (5%)	100	6.23	1.23%
	20 (20%)		21.48	1.48%
	50 (50%)		50.88	0.88%
ab	5 (5%)	0	6.13	1.13%
	20 (20%)		-	-
	50 (50%)		47.98	2.02%
abcg	5 (5%)	0	7.03	2.03%
	20 (20%)		22.41	1.41%
	50 (50%)		50.46	1.46%
	5 (5%)	20	3.97	1.03%
	20 (20%)		22.35	2.35%
	50 (50%)		50.84	0.84%
	5 (5%)	100	6.82	1.82%
	20 (20%)		19.07	0.93%
	50 (50%)		49.25	0.75%

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