ADVANCES IN DIGITAL SIMULATOR DEVELOPMENTS

FOR PROTECTIVE RELAY TESTING

M. Kezunović Texas A&M University U.S.A.

Abstract—This paper summarizes two digital simulator developments undertaken by Texas A&M University. One development was sponsored by the Electric Power Research Institute (EPRI) and was aimed at implementation of an open—loop, digital simulator for relay testing. The other development was sponsored by the U. S. Department of Energy—Western Area Power Administration (DOE—WAPA) and was aimed at implementation of a real—time digital simulator for relay testing. Both projects have resulted in prototype simulator configurations that were used to demonstrate some new concepts and applications.

Keywords: Digital Simulators, Relay Testing, Electromagnetic Transient Program (EMTP), Real-Time Simulation

INTRODUCTION

Digital simulators for relay testing have been used since the early 80's [1]. Until today, several open-loop designs have been introduced with various performance characteristics [2-3]. Real-time designs have also been implemented in the early 90's [4,5].

Development of the digital technology for simulators in the U.S.A. has been initiated in the mid-80's with one of the first designs being implemented by the Bonneville Power Administration (BPA) [2]. In the late 80's and early 90's, both EPRI and DOE-WAPA initiated independent simulator development projects. Texas A&M University was funded to carry out both of the developments.

This paper summarizes various aspects of these developments already described in a number of publications [6-16]. A brief description of the goals, as well as simulator hardware and software developments, is given for both projects.

EPRI PROJECT

Study Objectives

The initial study objectives were [5,13]:

· Development of Simulator Guidelines

- Application of EMTP and Digital Fault Recorder (DFR) Files
- · Specification of Test Cases

As a result of the initial study, that was completed in the Summer of 1992, an EPRI report summarizing the findings was published [10]. The report has covered detailed study of the following topics:

- · Digital Simulator Requirements
- · Application Guidelines for Relay Testing
- Digital Models of CCVTs
- · Study of CT Models
- · Examples of Digital Simulator Applications

In addition, a PC-based simulator design has been built and its operation has been demonstrated.

The project has been extended from 1992 until 1995 to include further simulator developments and relay testing applications.

Simulator Hardware

Simulator hardware characteristics are described in several papers [3,10,14]. A block diagram of the hardware is given in Fig. 1.

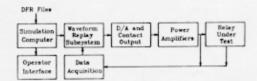


Fig. 1.Simulator Hardware

A simulation computer is used to generate transient waveforms, either through EMTP simulation or from DFR files. This computer has an elaborate graphical interface for the operator. It also communicates with a waveform replay subsystem.

The waveform replay subsystem is a separate computer system that is used for real-time waveform reconstruction. It feeds waveform samples into the D/A subsystem. It also generates contact data. At the same time, this subsystem interfaces to the data acquisition equipment which captures relay and simulator outputs.

The D/A and contact output subsystem is used to convert signal samples into analog waveform and contact signals. These signals are eventually used to feed relays for testing purposes.

The power amplifiers are needed to increase power of the analog waveforms to the levels present at the secondaries of the instrument transformers. Using the amplifiers, test signals with the characteristics very close to the ones the relay sees in the field are produced.

The D/A, digital I/O and power amplifier subsystems are packaged together in an I/O cabinet. The basic characteristics of the I/O cabinet design are given in Table I.

Table I. Basic Characteristics of the I/O Cabinet

ITEM	SPECIFICATION
# of Bits	16
Sample Rate	Fs=3.2 to 25 kHz
Output Imped.	Voltage Channels: $< 1\Omega$ Current Channels: $> 500\Omega$; DC to kHz
Anal. Bandwidth	DC→0.45 fs
Out. Sig. Range	Voltage Chann:> ±320Vpeak; ±0.2Apeak Current Chann:> ±160Apeak; ±100Vpeak
Anal. Chann.	12 Voltage + 12 Current*
Digit. Chann.	48 Input + 48 Output**
Channel Skew	< 1µs

- 3 sets of 4 voltage and 4 current channels
- ** 3 sets of 16 input and 16 output channels

Simulator Software

Simulator software characteristics are described in detail in reference [9]. A block diagram of the software is given in Fig. 2.

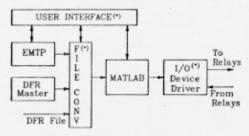


Fig. 2. Simulator Software

It shall be noted that some of this software is commercially available, while some of the software had to be developed. The software blocks marked by an asterisk are the developed ones. A brief description of the commercial packages i given below, while the new software developments are outlined next.

EMTP is a well known program for simulation of transients in power networks [17]. This package is quite complex and requires elaborate input data for modeling of power system faults. Extensions for instrument transformer modeling are needed when EMTP is used for relay testing [7,8].

MATLAB is a general purpose signal processing package which allows extensive signal parameter calculation and analysis [18]. This package provides the user with a high level command language which can be used to develop various applications.

DFR Master software was developed by DFR manufacturers to allow for viewing and editing of DFR files. Characteristics of these packages vary from vendor to vendor.

The application software that has been developed for this project has been organized into four main modules: User Interface, Signal Conversion, Signal Analysis and Signal Processing. Each module contains routines to perform specific tasks. The block diagram in Fig. 3 shows the various functions available in the software. The software was developed in MATLAB.

WAPA-DOE PROJECT

Study Objectives

The initial study objectives were [5]:

- Selecting a suitable commercial computer hardware and system software for simulator implementation.
- Selecting a suitable high precision, high power I/O interface.
- Developing a new real-time application software for generation of fault transients.
- Implementing a real-time interaction between digital simulator and I/O subsystem used for interfacing with protective relays under test.

The first task of selecting an appropriate commercially available computer system architecture was accomplished by running several benchmark programs on a number of different high performance computers. After an elaborate study was concluded, it was apparent that none of the low cost, high performance parallel architectures were suitable for the simulator application. The only remaining choice was to select a distributed computer architecture consisting of several low cost, high performance, sin-

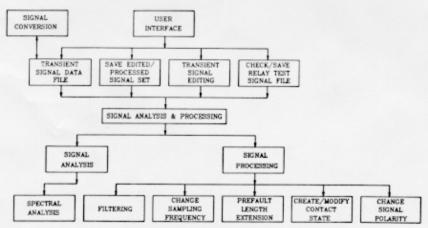


Fig. 3. Software Modules for Transient Testing

gle processor computers. Further evaluation led to the choice of IBM RISC 6000 computers in combination with Sonitech DSP boards.

The second task of selecting a high precision, high power I/O interface was accomplished by utilizing such a design developed under EPRI project RP 3192-01. This equipment was manufactured, under EPRI sponsorship, by a commercial vendor.

The task of developing a real-time simulation software led to an in-house implementation of an EMTP-like software customized for high speed execution. A number of new numerical approaches and algorithms were introduced to represent and simulate power system components [12,16].

Finally, implementation of the real-time interaction between the digital simulator and the I/O interface was carried out by developing special I/O cards.

The DOE-WAPA project has resulted in an implementation of a real-time simulator that was delivered to WAPA in March 1994.

Simulator Hardware

Simulator hardware characteristics are described in several papers [5,11,15]. A block diagram of the hardware is given in Fig. 4.

As can be observed, it is a distributed system architecture with two IBM RISC computers and two Sonitech DSP boards, each dedicated to a particular processing task. The task allocation is such that the user interface interaction is performed off-line. The real-time interactions between power system network, instrument transformer, and circuit breaker simulations are achieved by a careful coordination among tasks executed on IBM RISC 6000/580 and Sonitech DSP computers. Furthermore, real-time interaction between the simulator and the relay under test is implemented through the high precision, high power interface which outputs analog waveforms and contacts to the relays, and takes the trip signals from the relays back into the simulator.

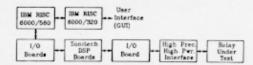


Fig. 4. Real-Time Digital Simulator Architecture

Hardware and system software are commercially available products. The only exceptions are some communication support software routines written as device drives for the three I/O boards developed by Texas A&M University. In Fig. 4, these boards are identified as the I/O board blocks. The I/O board block between the IBM RISC 6000/580 and the Sonitech DSP computers consists of two interface boards, each connecting the respective computers to the parallel communication link between them. The I/O block connecting Sonitech DSP boards to the high precision, high power interface contains one interface board that converts parallel data coming from the DSP board into a serial communication

format used to send data out to the relay interface.

The high precision, high power I/O interface is packaged in a 19" cabinet housing D/A conversion boards, as well as up to 4 current and 4 voltage amplifiers. The D/A boards and voltage amplifiers were designed by Texas A&M University, while the current amplifiers were selected from a standard product line of TECHRON, a division of Crown International. A cabinet prototype was assembled and extensively tested by Texas A&M University. After that, a commercial version of 3 cabinets was manufactured and used in the WAPA simulator configuration.

Simulator Software

Application software has been developed by Texas A&M University, and customized for real-time application. A block diagram of the application software is given in Fig. 5.

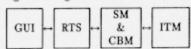


Fig. 5. Application Software

The GUI block diagram designates an elaborate graphical user interface developed to enable the operator to interact with the rest of the application software in a very simple and straight forward way. The GUI software resides on the IBM RISC 6000/320 computer.

The RTS block represents the real-time system. This application software package consists of a real-time transient network simulation module which enables changes of the network topology in real-time as a trip signal from the relay is received [12]. The list of component models supported by this module is given in Table II. The RTS resides on the IBM RISC 6000/580 computer.

The SM&CBM block consists of the System Manager (SM) and Circuit Breaker Modeling (CBM) software modules. These modules reside on one out of the four DSP chips available on the two DSP boards. The SM module coordinates real-time interaction related to data transfers between RISC 580 computer and other DSP chips. This includes transfer of waveforms and contacts going out of the RISC 580 computer to the relays, and contacts returning from the relays through the DSP chips. The CBM module incorporates a full timing logic of a breaker. Each of the relay trip signals goes through this timing logic before they are transferred to the RTS module eventually causing a change in the net-

work topology.

· Surge arresters

Table II. Network Components of the RTS

ullet Uncoupled branches: R, L, C and $R-L$
Coupled R - L branches

Constant parameter overhead transmission lines
• Transmission lines with frequency dependent parameter
Voltage sources
• Faults
• Relays
Switches and Circuit Breakers

· Series capacitors with MOV protection

The Instrument Transformer Model (ITM) block is related to the detailed models of instrument transformers. This block consists of 3 sets of modules, each residing on one of the remaining DSP chips. Each of these modules is comprised of 3 CCVT and 3 CT models, which are all together executed for each time step. This approach to the ITM software implementation enables full modeling of up to 18 instrument transformers in a three terminal protective relay testing configuration.

All of the software residing on the IBM RISC machines is written using the standard C language. This software is portable to any UNIX-like environment, and in particular, it is upward upgradeable for any new set of IBM machines that may become available in the future. The software written for the DSP chips is in the assembly language and can run on any future upgrades of the TI C40 chip based boards.

CONCLUSIONS

Based on the similar developments discussed in the paper, the following conclusions can be drawn:

- Advanced digital simulators for relay testing can be designed using readily available software/hardware technology
- Open-loop simulator design requires extensive developments of user software
- Real-time simulator design requires new design of the real-time electromagnetic transient program
- Both simulator developments require new design of the I/O cabinet as well as custom designed hardware and software for interfacing I/O cabinets to the simulation computer.

ACKNOWLEDGEMENTS

The simulator developments were funded by EPRI under Contract # RP 3192-01, DOE-Western Area Power Administration (WAPA) under contract #FC 65-90WA 07990 and by direct co-funding contributions to EPRI from the following utilities: Houston Lighting & Power Company (HL&P), FPL Company, WAPA, Pacific Gas & Electric (PG&E). Texas A&M University has provided co-funding as well. The following individuals have contributed to the various technical concepts presented: S. Nilsson, L. L.Mankoff, F. Phillips, M. Wilhelm (EPRI); S. M. McKenna, J. Bladow, D. Hamai (WAPA); C. W. Fromen, D. R. Sevcik (HL&P); B. A. Pickett (FPL); J. Esztergalyos (BPA); D. Tziouvaras (PG&E). Close to two dozen postdoctoral fellows, graduate students and research staff at Texas A&M University have carried out the development activ-

REFERENCES

- A. Williams, R. H. J. Warren, "Method of Using Data from Computer Simulation to Test Protection Equipment," *IEE Proceedings*, Vol. 131, Pt. C, No. 7, November 1984.
- [2] J. Esztergalyos, et. al., "Digital Model Power System," *IEEE Computer Applications in Power*, Vol. 3, No. 3, July 1990.
- [3] M. Kezunović, et. al., "DYNA-TEST Simulator for Relay Testing, Part I: Design Characteristics," *IEEE Trans. on Power Delivery*, Vol. 6, No. 4, October 1991.
- [4] P. G. McLaren, et. al., "A Real-Time Digital Simulator for Testing Relays," *IEEE Trans. on Power Delivery*, Vol. 7, No. 1, January 1992.
- [5] M. Kezunović and S. M. McKenna, "Real-Time Digital simulator for Protective Relay Testing," IEEE Computer Applications in Power, Vol. 7, No. 4, July 1994.
- [6] L. L. Mankoff, M. Kezunović, "Protective Relay Workstation: Applications of a Digital Simulator," Texas A&M Relay Conference, College Station, April 1991.
- [7] M. Kezunović, et. al., "Digital Models of Coupling Capacitor Voltage Transformers for Protective Relay Transient Studies," *IEEE Trans.* on Power Delivery, Vol.7, No. 4, October 1992.
- [8] M. Kezunović, et. al., "Experimental Evaluation

- of EMTP Based Current Transformer Models for Protective Relay Transient Study," *IEEE* PES Winter Meeting, Paper No. 93WM 041-4-PWRD, Columbus, February 1993.
- [9] M. Kezunović, et. al., "Advanced Signal Processing and File Management Software for Relay Testing Using Digital Simulators," 11th PSCC, Avignon, France, September 1993.
- [10] M. Kezunović, et. al., "Protective Relay Workstation – Application of Digital Simulator for Protective Relay Studies," Electric Power Research Institute RP 3192-1, Phase I Final Report TR-102781, Palo Alto, California, October 1993.
- [11] M. Kezunović, et. al., "New Digital Simulator Design for Protective Relay Testing," Texas A&M Relay Conference, College Station, March 1994.
- [12] M. Kezunović, et. al., "Transients Computation for Relay Testing in Real-Time," IEEE PES Summer Meeting, Paper No. 93 SM383-0 PWRD, Vancouver, British Columbia, Canada, July 1993.
- [13] M. Kezunović, et. al., "Use of Digital Fault Recorder Files for Protective Relay Evaluation," Fault Disturbance Conference, College Station, April 1991.
- [14] M. Kezunović, et. al., "DYNA-TEST Simulator for Relay Testing, Part II: Performance Evaluation," *IEEE Trans. on Power Delivery*, Vol. 7, No. 4, July 1992.
- [15] M. Kezunović, et. al., "A New Multiprocessor Architecture Implementation of a Real-Time Simulator for Power System Aplications," ISCA Intl. Conf. on Computer applications in Industry and Engineering, Honolulu, Hawaii, December 1993.
- [16] M. Kezunović, et. al., "Computing Responses of Series Compensation Capacitors with MOV Protection in Real-Time," *IEEE PES Summer Meeting*, Paper No. 94SM 400-02 PWRD, San Francisco, July 1994.
- [17] Electromagnetic Transients Program (EMTP) Rule Book, EPRI EL-6421-I, Vol. 1, 2, Research Project 2149-4, June 19889.
- [18] PC-MATLAB User's Guide, The MathWorks Inc., Sherborn, Massachusetts.