

International Conference on Large High Voltage Electric Systems

112 houlevent Haussmann - 25/06 Paris

1986 Session - 27th August-4th September

34-11

Pref. Subj. 2

APPLICATION OF DIGITAL COMPUTER TECHNOLOGY TO THE IMPLEMENTATION AND TESTING OF AN INTEGRATED SUBSTATION PROTECTION AND CONTROL SYSTEM

M. KEZUNOVIĆ*, S. KRESO, P. VUJOVIČ

Energoinvest Company

(Yugoslavia)

B. PERUNIČIĆ, S. SADOVIĆ University of Sarajevo

Summary

An Integrated Microprocessor - Based Substation Control and Protection System is described in this paper. Also, the main characteristics of digital simulators to be used as testing tools for protective relaying and control functions are outlined.

The Integrated System presented consists of several subsystems: Distance Relay, Transient Recorder, Local Automatic Control Subsystem, Communication Serial Multidrop System Link, Supervisory Subsystem, Fiber--optic Point-tr-pointLink. The following issues related to the Integrated systems are considered: Design philosophy and functions, System architecture, hardware, software, communications, algorithms, system testing and future activities.

Digital Control, Digital Protection, Fault Recording, Fiber Optics, Digital Simulators.

1. INTRODUCTION

Application of Microprocessors to development of substation Control, Protection and Data Acquisition Systems started in the mid 70's [1]. Use of the LSI technology enabled several design improvements to be achieved as well as some new concepts to be introdu-

Concept of the Integrated Substation Control and Protection System was promoted in the late 70's and first development projects were completed in the mid 80-es [2]. Major claims for Integrated system advantages were related to improvements of the cost/performance characteristics of the solutions.

A specific solution of an Integrated System is described in this paper [3]. Several design requirements as well as the solution characteristics are ed . Major emphasis of the discussion is placed on the issues of integration of control and protection functions in one system. Some initial test results are presented and several problems related to the design of digital simulators for Integrated System testing are analysed.

System design philosophy and functions are outlined first. Then, the following characteristics of the Integrated system are discussed: System architecture, hardware, software, communications and supervisory level, algorithms. Issues related to system testing and future activities are presented at the end.

2. DESIGN PHILOSOPHY AND FUNCTIONS

In order to investigate the issues of the Integrated System design philosophy and functions, speci-fic methodology for problem analysis was utilized [4]. The major conclusion was that the Integrated concept is quite attractive taking into account op-timization of the system cost/performance characteristics. The following discussion gives an overview of the system design requirements and implementation characteristics.

2.1. Design Philosophy

A detailed analysis of the design philosophy problem shows that there is a number of different design app-roaches that can be implemented when microprocessor technology is used to develop substation control, protection and data acquisition equipment (5). If the Integrated concept is considered then there are several arguments that can be developed to promote a different approach to implementation of the Integrated concept [6].

Design philosophy undertaken in the implementa-tion described in this paper is based on the following criteria:

- type of the substations
- implementation approach
- engineering design testing and maintenance
- overall power system control and protection
- introduction of new concepts and functions.

When various types of substations are considered it can be concluded that different control and protection coordination requirements can be defined. This of course has an impact on the Integrated System architecture, allocation of functions and data flow requirements (5). Therefore it was decided that a modular design of an Integrated system should be developed to enable adequate configuration for a particular substation type.

It was also concluded that microprocessor-based systems can be utilized in both old and new substations. This means that the new equipment has to have 34-11

both canability to interface to the old equipment and to be easily expanded. From this conclusion a requirement emerged that the system modules should correspond to the conventional equipment and that various interface capabilities should be provided. This would enable adequate implementation approach depending upon the existing equipment in the sub-

Engineering design requirements of the conventional control, protection and data acquisition equipment are quite different among themselves. However, use of the microprocessors to implement those functions should change this practice of different engineering approaches, methodologies and tools. Hence, a requi-rement for development of a unique approach to engineering design was also part of the Integrated System development philosophy. This called for the use MICROSTORE of the uniform hardware, software, communication and interface techniques throughout the system.

Integrated system testing and maintenance was considered extremely important issue when the design phi-losophy was considered. Again, a unique approach to this problem at the system level is considered as a requirement. This called for development of adequate system software and interfaces as well as for development of special digital simulators for this pur-

When an Integrated concept was studied, it was evident that its implementation using microprocessor technology had a bearing on the overall concept of power system control and protection. It was considered that the Integrated System should act as a RTI for the SCADA system and in the future some of the Energy Management System functions could be redistributed to the Substation Integrated System level 17,83. Therefore, an interface to the SCADA System is also considered as a requirement.

Finally it was recognized that implementation of the microprocessor-based control and protection equipment as well as the implementation of the Integrated concept are a big departure from the conventional designs. Therefore, it was decided that the microprocessor-based Integrated system development at hand should be gradual. This ended up as a require-ment that the Integrated System should be developed in two phases. Phase I is to include one represen-tative function from each of the control, protecti-on and data acquisition groups of functions.

2.2. System Functions

As it was mentioned, the Integrated System described in this paper represents the Phase I of the overall Integrated concept development. This Phase I system consists of the following subsystems:

- MICRODIR (Distance Relay)
- MICROSTORE (Transient Recorder)
- MICROLARTS (Local Automatic Control Subsystem)
- MICROCOMM (Serial Multidrop Communication Subsysten)
- MICROSUPER (Supervisory Subsystem)
- MICROFIBO (Fiber optic point-to-point link)

Table 1. gives list of the specific functions and their requirements as they relate to each of the mentioned subsystems.

3. SYSTEM ARCHITECTURE

This section gives description of the architectures of each of the subsystems. Data flow and system interfaces are also discussed. It should be noted that a study of number of different system architectures was performed before the selection of the given architecture [5,9].

TABLE 1: INTEGRATED SYSTEM FUNCTIONS AND REQUIRE-

MICRODIR

- Functions: fault detection, classification, verification
- Zones: 3 forward, 1 reverse
- Characteristic: quadrilaterale - Starting element: underimpedance
- Features: voltage memory, crosspolarizing logic, compensation for zero current, extension of Zone I
- Sampling frequency: up to 1 kHz
- Tripping time: 30 ms for Zone I

- Functions: transient recording, sequence of events, operator measurements
- Prefault data: 5 periods Post fault data: 30 periods
- Sampling frequency: up to 2 kHz
- No. of records on the cassette: 10
- Starters: analog, digital, manual, automatic

MICROLARTS

- Functions: automatic switching sequences, LTC control of 2 transformers in parallel
- No. of digital I/O: 128/128
- No. of analog inputs: 4 currents, 4 voltages
- Sampling frequency: up to 0.5 kHz

MICROCOMM

- Type of comm. protocol: CSMA/CD Controllers: Ethernet

- Speed: 1 MB/sec No. of drops: up to 10 Length: up to 500 m

MICROFIBO

- Frequency bandwith: up to 2 kHz
- Modulation: PFM (pulse frequency modulation) Accuracy class: ±3%
- Noise to signal ratio: 60 dB
- Angle error between phases: ±10

3.1. Integrated System

Layout of the Integrated System architecture is given in Figure 1.

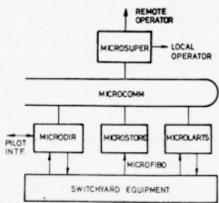


Figure 1. Integrated System Architecture

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As far as the data flow is concerned, it can be seen that the input data from the switchyard equipment is brought to the subsystems either via the fiber optic point-to-point link or via the conventional wiring. This data is processed in the MICRODIR, MICROSTORE and MICROLARTS subsystems. After the processing some switching outputs can be generated from MICRODIR and MICROLARTS subsystems to the switchyard. Processed data is further brought via the MICROCOMM communication subsystem to the MICROSUPER supervisory subsystem.

In the oposite direction, from MICROSUPER to the subsystems, the switching command actions for MIC-ROLARTS are transmitted.

Also, the testing initiation commands to all of the three subsystems are sent. Finally, operator initiated settings are also sent via the MICROCOMM to the three subsystems. Sempling synchronization is also sent that way.

Integrated system interfaces are of the two types: operator interfaces and substation equipment interfaces.

Operator interfaces are provided at the subsystem level as well as at the system level. Each of the interfaces contains operator dialog device and data presentation and recording equipment. Two operator dialog devices are provided at each of the interfaces. One device is standard operator panel with switches for settings and LEDs for signalization. Another operator dialog device is a RS232C compatible device (CRT or hand-held terminal). Data representation and recording equipment is different depending upon the subsystem function and those interfaces are described in the next section related to subsystem architecture.

Substation equipment interfaces include the following: switchyard interfaces, communication interfaces for pilot protection, SCADA system interface.

3.2. Subsystems

It should be noted that each of the subsystems is designed arround a general subsystem architecture given in Figure 2. The major differences are in the number and type of I/O units, CPUs, memory boards, communication controllers and peripherals.

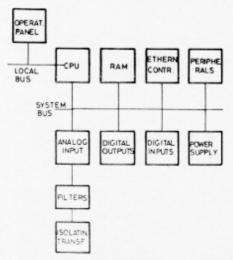


Figure 2. General Subsystem Architecture

MICRODIR consists of one CPU board, analog input board, isolating transformers and filter boards, digital 1/0 board and the communication controller board. It also contains pilot interface, autoreclose and out-of-step protection modules which are external to the microcommuniter part of the relay [10].

MICROSTORE consists of CPU, 512 KB RAM, analog input, isolating transformer, filter, starting detector, digital I/O and communication controller boards. It also has interface boards for cassette, ploter and printer peripherals.

MICROLARTS has two CPU boards, one analog input, RAM, isolating transformers, filter and communication controller board and several digital 1/0 boards. It also has interface boards for a printer.

MICROSUPER consists of one CPU board, two communication boards (a MICROCOMM controller board and a SCADA interface board), one mass memory interface board, one RAM board and interface boards for plotter and printer peripherals.

Finally, it should be also noted that each of the subsystems has the operator panel board which provides setting switches and signalling LEDs interfa-

4. RARDWARE

The Integrated System is designed around INTEL microprocessors and MULTIBUS system architecture.

4.1. Modules Characteristics

CPUs are 16 bit of the Intel 86/14 board type. PROM versions of the software are located on the CPU boards. RAM boards wary in size and modularity. The biggest size is 512 KB on one board, and the smallest is 32 KB on one board.

I/O boards are of the three types: analog imput boards, digital input and digital output boards.

Analog input boards are: isolating transformers, antialiasing filters and A/D converter board. There are two types of A/D converter boards. One type has A/D converters per channel and the other type is an "intelligent" board with one A/D converter per 8 channels and an 8-bit microprocessor on the board. This "intelligent" board has options for adjustments

of sampling rates and programmable gain amplifier circuitry (11]. A/D conversion is a 12 bit conversion with 16-bit word operation. Also, an analog input board is the analog detector board.

Digital input boards are optocoupler boards and digital detector boards. Digital output boards are relay boards.

Communication controller boards are of two types: Ethernet type and serial/perallel port boards.

Peripheral controller boards are: mass memory controllers, cassette controller, keyboard controller.

4.2. System Bus, Power Supplies and Casing

System buses used are Intel MULTIBUS and local processor bus of the iSBx type. CPU, Memory, 1/0 and peripheral boards are connected to the MULTIBUS. Operator panel boards are connected to the iSBx bus.

Power supplies are modular in design and cover the following voltage levels with adequate polarity: 5V, 12V, 15V and 24V. The input voltage is 110 or 220 V DC.

The prototype version of the system is housed in Intel ICS 80 casings with additional racks for some

I/O and peripheral boards.

5. SOFTWARE

Software includes application and system software. Programming languages used are assembly language for critical real time applications and PLM high level language for less time critical applications.

5.1. Application Software

Application software resides in the 16-bit CPUs and on the 8-bit A/D board CPU. Each time at the powerup situations the application software is initiated and is executed until the main action in the system is performed. After that the system is reset and the software is initiated again. A system reset can be also operator initiated.

Flow charts for MICRODIR, MICROSTORE and MICROLARTS software are given in Figure 3, 4 and 5.

5.2. System Software

This software consists of the operating system, monitors, testing software and special routines software such as real time clock software, sampling synchronization software, system communication software, and operator interface software.

Operating systems are used in the MICROLARTS and MICROSUPER subsystems and are based around RMX 86 like operating system. Special monitors are designed for operator interface dialogs. Testing software is quite elaborate and contains special routines for start-up, periodic self-checking and long-term maintenance testing.

Real-time clock and sampling synchronization software is used in all of the subsystems. Special communication drivers software is developed for exchange of the messages over the ETHERNET communication system. Special drivers are also developed for various peripherals which are part of the operator interfa-

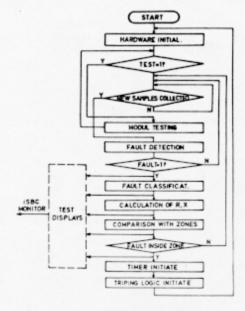


Figure 3. MICRODIR Software Flow Diagram

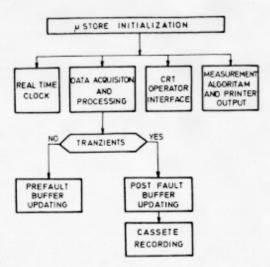


Figure 4. MICROSTORE Software Flow Diagram

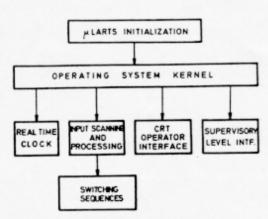


Figure 5. MICROLARTS Software Flow Diagram

6. COMMUNICATIONS AND SUPERVISORY LEVEL

6.1. Communications

The Integrated system has three types of communication subsystems: serial high speed system multidrop link, parallel processor bus and point-to-point fiber optic link.

First studies related to the multidrop serial link were simed at a custom design scheme (12). A latter decision was to implement a standard scheme. The multidrop link is ETHERNET based Local Area Network type of arrangement. ETHERNET controllers used are simple controllers with no processors on it. Software drivers are executed on the main CPUs in the subsystems. During this execution the application software is suspended. Therefore, the communications are performed at the times when application software suspension is not so critical.

Parallel processor buses represent the system bottleneck. A careful design was implemented which provided a time-slot type of synchronization of the

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MULTIBUS transfers so that required messages could be exchanged. This synchronization is implemented using both hardware and software techniques.

Point-to-point fiber optic link is implemented by providing the isolation and filtering hardware at the instrument transformer level. This circuitry provides 2 10V signal which is converted to the optical signal and transmitted to the subsystem inputs. This signal is then again converted into ± 10V electrical signal which is further processed by the

6.2. Supervisory Level

The MICROSUPER subsystem is the supervisory level and it is extremely important because it provides system interfaces between the local end/or remote operators and the subsystems.

All of the operator interfaces that are provided at the subsystem level (MICRODIR, MICROSTORE and MIC-ROLARTS) are also provided at the MICROSUPER subsystem. The ETHERNET communication software at this level is organized in such a way that all of the messages from the subsystems are received in the order of their arrival. Also, a message is provided on the CRT to notify the operator of a new message arrival.

At the MICROSUPER level there is a local SCADA database which enables appropriate organization of the Integrated system supervisory data. A special software is needed to interface this data base to the overall SCADA data base at the master station

Testing software is also initiated from the MICRO-SUPER level. Operator settings and commands could be also entered at this level.

7. ALGORITHMS

7.1. Integrated System Algorithms

Algorithms used in the system can be divided into two groups: analog input signal processing algorithms and digital input signal processing algo rithms. Analog input signals are processed to calculated values of current, voltage, impedance, active and reactive power and energy. Calculated values can be either peak values, instant values or RMS values. Digital input signals are processed to perform contact status filtering, indication of alarms and status information, determination of sequence of events and logical processing for execution of automatic switching sequences.

Distance relaying algorithm consists of the fault detection, fault classification and fault verifica-tion procedures. Both fault detection and fault classification procedures are performed using samples and amplitude values [13]. Amplitude values are calculated using a fast 3-sample algorithm [14]. Fault verification algorithm is based on solution of a differential equation which provides expressions for calculation of R and X parameters [15].

Transient recording algorithm collects the sampled values and organizes them into appropriate pre-fault and post-fault buffers. Additional processing of digital inputs is performed to record sequence of events corresponding to transient records. In the normal situations of the power system Transient Recorder collects samples and calculates measured values of current, voltage, active and reactive power. Algorithms to calculate those values are based on the Walsh transform [16].

Automatic control algorithms are performed based on samples of analog and digital input signals. Similar

algorithms as in the two previous subsystems are used to process analog input signals to determine appropriate values for the LTC control algorithm. An algorithm is also provided to perform logic operations for automatic switching sequences.

7.2. Algorithm Studies

Several algorithm studies are performed to determine characteristics of the various analog input signal processing algorithms proposed so far for protective relaying [17]. Those studies include Generalized algorithm form study, Error analysis study, Algorithm classification study and Algorithm comparison study.

Study of a Generalized Algorithm Form should define a common form to represent all of the known algorithms [18]. Certain parameters of the form are adjustable to take into account specific requirements of the unique properties of some of the algorithms. This study enables comparison of the various algorithm forms proposed so far in order to define a unique form for number of the similar algorithms.

Error analysis study gives analysis of the three sources of errors in the protective relaying algorithm based on the solution of a differential equation [19]. The three sources of errors are: trans-mission line model error, R and X parameter estimation error and the sampling rate error.

Algorithm classification study shows that there are two major groups of algorithms [20]. One group is based on a set of algebraic equations with two unknowns, namely distance of the fault and fault impedance. The other group is based on the identifi-cation methods for determining the fundamental harmonic using either recursive or nonrecursive methods

It was shown that first method requires careful filtering procedures while the second method has an inherent filtering feature. It is also shown that the first group of algorithms depends on the transfer function of the instrument transformers as well as on the sampling synchronization while the second group depends only on the transfer function characteristic at the fundamental harmonic frequen-

Algorithm comparison study includes analysis, syn-thesis and evaluation of digital protective relay-ing algorithms [21]. A list of the algorithms with typical evaluation figures is given in Table 2. A Criterion for evaluation is given by the following

MAXDIST - | MEANING - MEAN VALUE | + | COEFF - STD |

where: MAX DIST

MEAN IMP - 61.27%, mean value of the actual fault impedance

MEAN VALUE - mean value of fault impedance calculated based on measured

values

- fault impedance standard deviation calculated based on mea-

sured values

- 2.58 , for probability of 99% (normal distribution) COEFF.

It should be noted that the algorithm ranking based om a simple criterion such as the mean value or stan-dard deviation can be quite misleading and therefore a more complex criterion given above was defined.

TABLE 2: TYPICAL TEST RESULTS FROM ALGORITHM STUDY

LIST ALGORITHMS USING-24(S/C)	FILTER 0.320(KHZ) CUTOFF PROBABILITY = 99.001		MEAN IMP. 61.27% COEFF. = 2.580
TIME-POST FAULT 1.5-2.5T			
ALGORITHM	MEAN VALUE	STD.	MAX. DISTANCE
1. McInnes-Morrison DW25T	60.75	0.85	2.70
2 McInnes-Morrison DUE ST	60.74	1.31	3.92
3. Breingan et all.	60.78	1.45	4.24
4. Kalman filter	63.87	0.67	4.33
4. Kalman filter 5. Lobos - Koglin DW = 4S	59.22	1.08	4.83
6. Bornard et all. DW25T	62.54	2.08	6.63
7. Bornard et all DWs.ST	52.55	2.25	7.07
8. Fourier an. DW = 1T 9. Brooks DW - OPT.	61.28	4.07	10.51
9. Brooks DW - OPT.	59.13	4.17	12.91
10. Algorithm "K-K" DW = 45	59.21	4.75	14.30
11. Gilcrest et all.	60.98	6.54	17.17
12. MSE DIFF. DW - 5T	60.98	6.82	17.87
13. Gilbert - Shovlin DW - 3S	59.15	6.48	18.85
14. MSE DIFF. DW 25T	60.78		
15. Hope et all correlat.	47.74	4.07	24.02
16. Luckett et all.			28.04
17. MSE FORM. DW 25T	64.12	11.41	32.29
17. MSE FORM. DW =.25T 18. Mann - Morrison	60.80	17.30	45.11
19. Fourier an. DW5T	61.07	51.52	133.13
20. Walsh an. DW - 175		0.00	******
	P		"y_y" - Yazunanii

MOTE: DW - data window MSE - mean square error DIFF - different. eq. FORW - forward sampling "K-K" - Kezunović, Kraso algorithm

8. SYSTEM TESTING

8.1. Test Results

The Integrated System is now in the stage of laboratory and field testing. Functional tests are being performed. Type test will be also performed in the near future. Further testing will be performed using digital simulators and analog simulators.

Features of the digital simulator will be described below. Analog simulator is a scaled physical power system model with rotating machines. Field testing will be performed in the High Power Lab and in a Substation environment.

Results of the tests performed so far show that all of the major functional requirements are satisfied. Further testing is to prove that all of the IEC standard tests are satisfied as well. Also, future tests will be performed to analyse system behaviour in various transient situations in the Electric Power System.

8.2. Digital Simulators

Two digital simulators, an analog signal and a digital signal simulators, are being developed as well.

Analog signal simulator is a computer based simulator which is capable of simulating transients of the voltages and currents in the network. There are three major portions of the simulator: a VAX computer to simulate the transients, a D/A computer to generate the analog signals and the power amplifiers to obtain the required power levels of the signal.

As of now, the computer programs are being developed to simulate transients in the network, behaviour of the instrument transformers and behaviour of the antialiasing filters. All of the programs are executed on a VAX 750 computer.

Two different programs are used to simulate the transients in the network: EMTP from UBC and a Frequency Dependent Parameters Program E23J. The EMTP is quite convenient for analysis of the nonlinear

elements as well as time dependent sequences of events. However the other program, based on the methof Fourier transform enables representation of frequency dependence of both lumped and distributed parameters [23].

The approach taken is such that the basic studies are performed using the EMTP, but the frequency dependence is taken into account using the other program. The simulation approach is such that the studies are performed by both programs and the results are compared. The best fit of the two simulations enables determination of the frequency for which an equivalent network is defined for further studies using the EMPT.

There are two sets of programs for instrument transformer studies: the current transformer programs and the voltage transformer programs. Those programs enable simulation of the transient behaviour of the instrument transformers of various types.

The current transformer programs, as they are being developed in the first step, take into account the nonlinear magnetizing effects.

The voltage transformer programs for CCVT simulation provide that transformer accuracy in transmitting the high frequency transients is taken into account [22]. The programs are based on equivalent transformer models which contain winding stray capacitance and Frequency dependent magnetic losses.

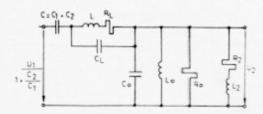


Figure 6-a. CCVT Equivalent Network

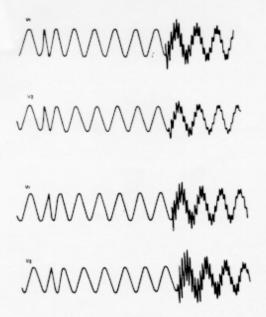


Figure 6-b. U, and U2 Transients

Figure 6 gives same results of theoretical and experimental study of a particular type of a CCVI. Figure 6-a gives one of the equivalent networks for a CCVI characteristics study. Figure 6-b gives record of the V_1 and V_2 transients obtained using injection method superimposing different harmonics. Figure 6-c gives example of theoretical and experimental determination of the frequency response characteristic for particular CCVI with constant parameters.

Antialiasing filters are simulated using a computer program which enables decimations of the input samples (21). Various types of filters of different order and various sampling rates can be simulated using this program.

Digital signal simulator is a different set-up designed around a microcomputer. This simulator generates various logical states which correspond to status contacts of the switching equipment, voltage regulators, automatic reclosing devices and protective relaying equipment.

9. FUTURE ACTIVITES

It should be noted that the near future activities will be in the area of system testing. A number of different laboratory and field tests are yet to be performed. It is expected that the Phase I system testing will be completed by the end of 1986.

Another group of activities, which will be performed in parallel to the testing, is the industrial packaging activity. This activity assumes replacement of all of the OEM boards with the in-Louse produced boards. Also, the in-house development should provide boards, casing and connectors which satisfy the European industrial standards.

Yet another activity is completion of the simulator developments.

Finally, a number of studies have been and will be performed related to the cost/performance characte-

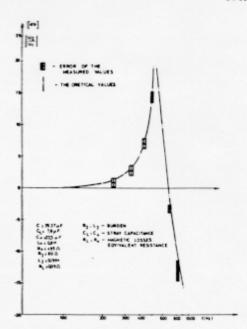


Figure 6-c. Frequency Response Function

ristics of the system. It is evident that the Integrated concept provides a number of advantages in this respect but more precise quantitative methods should be defined to take into account various situations in which the Integrated System can be applied.

10. CONCLUSIONS

Several conclusions can be drawn:

- Integrated control and protection system concept is feasible and implementation using the microprocessor technology provides improvement in the cost/ performance ratio.
- Am Integrated system design philosophy which assumes the protective relaying function integration using the same hardware and software principles as in the rest of the system seems to provide full adwantages of the Integrated concept.
- Future activities in the area of system testing, industrial packaging, simulator development and cost/performance studies are extremely important for final promotion of the Integrated System developed.

ACKNOWLEDGEMENTS

The authors wish to recognize contribution of colleagues at the Institute for Control and Computer Sciences who participated in the development work.

The authors acknowledge the funding support for the project which was provided by the Science Foundation of the Company, Factory for Secondary Equipment and the Science Foundation of the Republic Bosnia and Hercegovina.

The authors also gratefully acknowledge funding support from the funding agencies National Science Foundation from the USA and SIZ Nauke BiH from Yugoslavia made available to U.S.-Yugoslav Joint Board on Scientific and Technological Cooperation for the algorithm study. Also participation of Dr. J.T. Cain from University of Pittsburgh, USA is acknowledged related to the algorithm study.

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