DYNA-TEST Simulator for Relay Testing Part I: Design Characteristics

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Abstract - *This paper describes a new digital Dynamic Testing (DYNA-TEST) Simulator developed for protection relay applications. This simulator is capable of producing voltage and current transients that correspond to actual fault events in the power systems. Fault transients are generated either by simulating power system faults using an Electromagnetic transient program or by replaying records of fault signals captured in substations by digital fault recorders. These signals are used to test protection relays. Such an approach to relay testing is quite new and represents a major improvement over steady-state testing, which is the common practice in utilities today.*

Keywords: Digital simulator, relay testing, power system modeling, CT and CVT modeling.

INTRODUCTION

Present utility practice for protection relay testing is to use portable test-sets capable of producing steady-state test signals. A major advancement in this practice over the last 20 years was the introduction of computer-based test-sets with elaborate user interfaces and automated test features [1, 2].

Recent evaluation of the utility test practice has indicated that steady-state tests are not sufficient if the full behavior of a relay design is to be evaluated [3]. Some studies have also indicated that a detailed relay performance evaluation requires test signals that closely correspond to the actual fault signal [4, 5].

A number of different simulator designs capable of generating fault transients were developed in the past. Those designs include analog physical models of a power system, hybrid electronic designs and digital simulators [6, 7, 8]. These simulators can be used for dynamic relay testing, but their cost prohibits wide use in a utility environment. Because of that, these simulators were primarily used by the relay manufacturers and research organizations. Some of the latest designs are quite powerful and represent an excellent tool for relay testing and evaluation [9].

Recent advances in hardware and software development have enabled implementation of a new approach to utility practice in protection relay testing [10]. The new digital simulator is less expensive then analog or hybrid ones, and can be used for a number of common test applications found in a utility environment [11].

This paper provides the implementation details of the DYNA-TEST Simulator. First, digital simulator design with a new capability of supporting various test configurations is described. Generation of test signal files is discussed next. Use of the simulator in relay testing is outlined at the end.

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DYNA-TEST SIMULATOR DESIGN

Simulator Architecture

Details of the system architecture are shown in Figure 1.

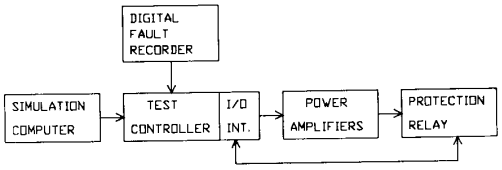

Figure 1. System Architecture

As can be observed from Figure 1, there are two sources of test signals. One is a simulation computer, which hosts the fault simulation program. The other is a Digital Fault Recorder (DFR), which makes records of the fault signals in a substation.

Both sources provide their signals in digital form, enabling easy file transmission to the test controller. The controller itself is mainly in charge of analog test signal generation. This is done through the dedicated D/A converter interface followed by the appropriate interpolation filters. These analog signals are then fed to the power amplifiers in order to increase their power level. Finally, test signals are injected to the relays. The controller also has a dedicated digital I/O interface used to communicate contact signals which are also needed and/or generated by the relays.

Hardware Characteristics

The hardware consists of the computer equipment, controller I/O interface and power amplifiers. Digital fault recorders and protection relays are external devices provided by the user and they are not a part of the DYNA-TEST Simulator design.

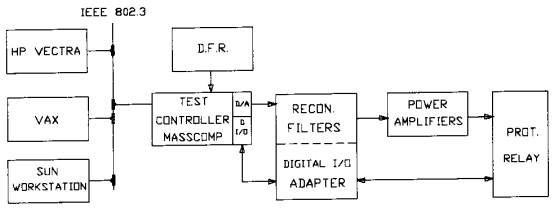

Figure 2. DYNA-TEST Hardware Configuration

Computer Equipment. Computer resources can be centralized in a single machine or distributed to several machines over the network. The choice will depend on the capability of an individual computer to run both, the fault simulation program and the real-time controller software. The actual DYNA-TEST computer configuration is shown in Figure 2.

As can be observed from Figure 2, DYNA-TEST Simulator provides several choices for the fault simulation computer. The reason for this was a design goal to support a wide range of computer requirements specified by different vendors of the fault simulation program. This configuration also enables different versions of DYNA-TEST Simulators to be implemented and tested. The most suitable simulator design for field applications is the one where the controller is used to run the fault simulation program as well. This is a portable version of the DYNA-TEST Simulator which consists of only one computer. Another portable option is to have the fault simulation computer located in the utility offices, and connected via modem to the controller computer located in a substation. The test files generated by the simulation can than be down-loaded to the controller upon request. The controller itself shall be equipped with an extensive pre-recorded fault simulation library so that remote fault simulations will be limited only to special situations.

Controller I/O interface. This interface provides connection of the controller with power amplifiers and the relay under test. The functional block diagram of the proprietary interface designed for the DYNA-TEST Simulator is shown in Figure 3.

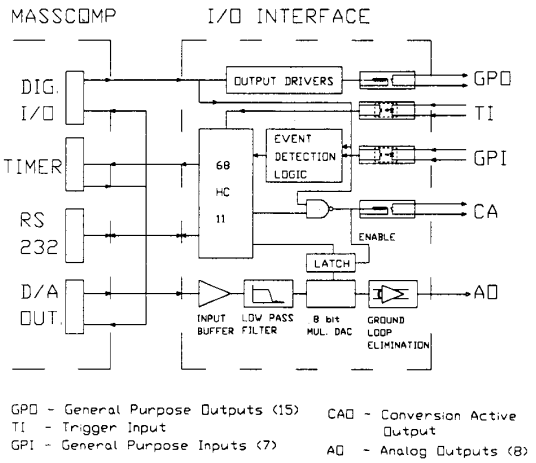

Figure 3. DYNA-TEST Simulator I/O Interface

This interface provides a high quality analog signal conditioning, event logging on 7 digital inputs, 16 digital outputs, and galvanic isolation of all digital inputs/outputs.

Analog signal conditioning includes: input signal buffering, low pass signal filtering, analog filter offset compensation, digital control of the analog channel gain (256 steps), and output signal buffering with additional ground loop elimination. The D/A converters are housed in the controller, and provide 8 synchronously clocked 12-bit channels.

A dedicated microcomputer is used to provide the I/O interface integration. This machine performs event logging, providing the time measuring facility needed to monitor the relay operation. This approach off loads the system controller enabling all of it's resources to be used for on line test signal generation. The communication between I/O interface and system controller is accomplished by using the simple RS 232 serial line.

Power amplifiers. Three current (transconductance), and three voltage amplifiers are typically needed. Amplifier requirements considered in the DYNA-TEST Simulator design are given in Table I.

Preliminary investigation of the commercial market has shown that there are a number of different amplifier products that could be used for the DYNA-TEST simulator design. Detailed amplifier testing and evaluation is under way to determine precise amplifier characteristics to be used as a future reference for configuring DYNA-TEST Simulator to do the test on specific relay types.

Table I. Typical Power Amplifier Requirements

Design Features	Voltage Amplifiers	Current Amplifiers
Output Voltage	> 200 V	> 60 V
Output Current	> 0.1 A	> 140 A
Power Dissipation	> 30 W	> 400 W
Power Dissipation (200mS MIN)	> 30 W	> 4000 W
Frequency Response (+-0.2 dB)	D.C. to 7 kHz	D.C. to 7 kHz
T. H. D.	< 0.2%	< 1%

Software Tools

DYNA-TEST Simulator integrates a number of software packages as shown in Figure 4.

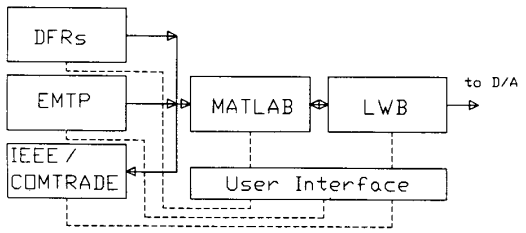

Figure 4. DYNA-TEST Simulator Software Organization

Most of the packages shown in Figure 4 are commercially available. An exception is the DFR conversion software which had to be developed specifically for this simulator.

DFR Conversion Software. As of today, all the Digital Fault Recorders use proprietary data formats for transfer and storage of recorded events. Therefore separate conversion programs are necessary for each DFR model/manufacturer. Conversions used in DYNA-TEST Simulator should provide paths from three commercially available DFRs to IEEE/COMTRADE common data format [12], MATLAB format [13], and LWB contiguous binary data format [14].

EMTPs. In order to facilitate the description of the DYNA-TEST Simulator, the program used for the simulation of electrical transients will be referred to as Electromagnetic Transient Program (EMTP) in a generic sense. It should be noted that none of the available programs is advocated here and the users could substitute their particular program titles for the generic title 'EMTP' used throughout this paper.

Simulation of power system transients can be done by using one of the programs available for this purpose. Currently there are a number of programs which simulate electrical transients [15, 16, 17, 18, 19]. DYNA-TEST Simulator is equipped to run all the EMTP versions cited above. Therefore, the user is free to decide on a particular program considering the available hardware at his/her laboratory.

The EMTPs (with one exception, [19]), in general, have not been developed exclusively for relay applications. Hence, the vast number of models and simulation procedures should be carefully examined to identify the necessary portions to be used for a particular application under study.

Filtering, Interpolation and Decimation. In order to simplify the overall DYNA-TEST Simulator hardware design while retaining the required high-precision output waveform, it was decided to fix the reconstruction system sampling frequency at 16 kHz. This frequency provides a 7 kHz signal bandwidth, sufficient for most transient tests, while using the standard audio-grade filter components. It also provides an easy upgrade to higher sampling rate standards (32, 48 kHz). While EMTP simulations permit generation of transients with an arbitrary sampling rate, the DFRs usually offer a limited set of fixed sampling frequencies. The available frequencies vary between different products/manufacturers, thus making the sampling rate conversion mandatory if the recorded data is to be used by the DYNA-TEST Simulator waveform reconstruction system. The conversion is performed by first finding the least common multiplier frequency, and then interpolating the incoming DFR signal in order to enable the subsequent decimation to 16 KHz. It is important to note that the interpolated signal has to be low pass filtered prior to the decimation, in order to preserve the original spectral contents. The detailed description of the sampling rate conversion process is given in [20]. It is important to note that this process preserves original signal bandwidth with 7 kHz being imposed as the upper limit by the utilized low pass filter.

MATLAB. General purpose signal processing and analysis is performed by means of the MATLAB software package. This versatile tool is used for frequency domain analysis as well as test signal parameter calculations such as harmonic power, line frequency, symmetrical components, RMS values, and phasor components. This package is primarily intended for advanced use requiring a highly efficient numeric analysis environment. It provides extensive plotting and hard-copy capabilities as well.

LWB. Laboratory Workbench provides the means for simple D/A conversion and digital output control. It also provides all the drivers necessary to control the MASSCOMP computer I/O hardware. The LWB package operates under the Real Time UNIX operating system, providing real time transfer of simulation data directly from the system hard-disk. It controls the synchronized operation of the built in timer, six D/A converters and 16 digital output lines.

GENERATION OF TEST SIGNAL FILES

Simulated Data

Test signals can be generated for a given system configuration and disturbance by using the EMTP. The procedure involves two steps: modeling of the power system and instrument transformers; fault simulation.

System modeling. Modeling the entire power system for EMTP studies is quite involved. This is due to the highly detailed data required for each power system component. On the other hand, the effect of the system components remote to the point of disturbance may not be significant. Therefore, it is common practice to reduce the full system to a small size equivalent network before disturbance simulation. The equivalencing problem can be solved in two ways: (a) Constant frequency short circuit equivalent computation [21], (b) Frequency dependent network admittance calculation [22].

Frequency dependent equivalents represent the external system more accurately over a range of frequencies. The idea is to replace the external network by a lumped parameter network of R,L,C elements which will match the frequency response of the original network within a prescribed tolerance. Obtaining such an equivalent is quite involved; nevertheless, some of the EMTPs provide it as a built-in feature.

The constant frequency short circuit equivalents can be obtained much easier. Their accuracy however is limited to a single frequency and therefore they should be utilized with care. The steps for obtaining a constant frequency (60Hz) network equivalent are summarized below.

Step 1. Disconnect the study system from the remaining part to be equivalenced (external system). Assume that there are M boundary buses connecting the study system to the external system as shown in Figure 5.

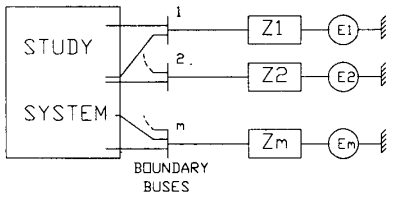

Figure 5. Power System Equivalencing Approach

Step 2. Apply a 3-phase to ground (3PH) and a single-line to ground (SLG) fault at buses 1,2,...,M; one at a time. Obtain fault currents I_f (3PH) and I_f (SLG) for each of the M buses.

Step 3. Compute

$$Z_i^{(+)} = Z_i^{(-)} = 1.0/I_f(3PH) \qquad i = 1, \ldots, M \tag{1}$$

$$Z_i^{(0)} = 3.0/I_f(SLG) - 2Z_i^{(+)} \tag{2}$$

Note that this method assumes that the coupling between the M boundary buses is negligible. If these couplings are significant, then the above procedure should be modified to obtain the transfer impedances between buses as well [17].

Once the system is reduced by using one of the abovementioned methods, then the study system should be modeled in great detail. It is recognized that the most important components in modeling for relay studies are transmission lines. The commonly used lumped-parameter nominal - π representations are no longer adequate for simulation of fast transients.

Among the available transmission line models in EMTP, two are best suited for transient simulations, namely the constant distributed parameter (CP) [23], and the frequency-dependent distributed parameter (FD) [24] line models.

The CP line model assumes that the parameters of the line (resistance, inductance and capacitance per unit length) remain constant over the entire frequency range. The zero and positive sequence impedances of lines are sufficient to model them as balanced CP lines.

The FD line model is used if the variation of the line parameters with frequency is to be taken into account. Data related to the tower geometry, conductor type and size as well as the earth's resistivity in the region should be available to develop the FD line models.

Since obtaining and using the FD line model is very involved, both in terms of data requirements and CPU time, it is used only for those lines which are of primary importance, i.e. the lines which are expected to influence the magnitude and/or shape of transients significantly. The remaining lines in the study system can be represented by using the CP line models.

Instrument Transformer (IT) Modeling. The steady state performance of ITs is well understood and it is specified by the ANSI/IEEE Standard [25]. However, Capacitive Voltage Transformer (CVT) is not covered by this standard. The transient behavior of ITs is also not covered by this standard.

The DYNA-TEST Simulator is intended for transient testing of protection relays. Consequently, the capability to simulate the transient behavior of ITs by development of accurate models suitable for DYNA-TEST Simulator is very important.

Transient performance of a CT is a complex, non-linear phenomenon. A number of papers have been written outlining different methods of investigation [26, 27, 28]. All of these approaches are based on analytical equations and the fault current is expressed as a function of DC and AC components. These approaches are not amenable for DYNA-TEST Simulator implementation and an existing EMTP model has to be used to represent the CT.

The EMTP does not have a CT model but it has a general TRANSFORMER model which is intended for voltage and power transformer representation. The CT can be represented using this model, but all the CT parameter values must be adjusted appropriately. The magnetizing branch's behavior is represented as a piece-wise linear flux-current characteristic obtained from the V–I saturation curve for the core.

The CT model using EMTP is shown in Figure 6. The model parameters are as follows: ratio, rated burden (VA), winding resistance and leakage inductance, and core V-I characteristic. All these values are commonly supplied by manufacturers and that is the advantage of using this model.

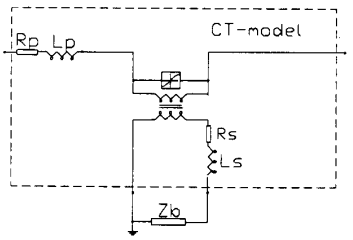

Figure 6. EMTP CT model

The CVT model has a complex structure and can be represented as shown in Figure 7.

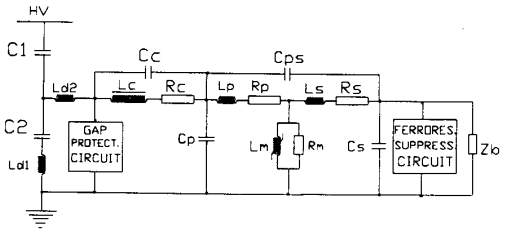

Figure 7. CVT Model

The CVT model consists of non-linear elements such as: compensating inductor, step-down transformer, ferroresonance suppression circuit inductor, and many circuits with L,C elements and gaps. All these elements can influence the CVT transient response and can considerably distort the secondary signal. Their representation results in a very complex CVT model requiring parameter data which is not easily available from the manufacturer. Detailed CVT modeling may require considerable computation time as well.

In order to simplify the CVT model, extensive analysis has been done. Some of the relevant conclusions concerning the CVT transient response are mentioned below. Experimental results supporting these conclusions are given in the accompanying paper [29].

Coupling Capacitor (CC), which is tuned with the compensating reactor and step down transformer leakage reactance, has significant influence in the lower frequency range.

Compensating Inductor (CI) has been represented in the CVT with its stray capacitance. Investigations in frequency domain show that the influence of CI stray capacitance on CVT frequency response is considerable at higher frequencies.

Step Down Transformer (SDT) impedances are measured with the windings short-circuited and open-circuited respectively. The influence of SDT winding stray capacitances on frequency response shows that the influence of C_{ps} and C_s on frequency response is small and can be neglected. Primary winding stray capacitance C_p is much higher than C_s. Its influence on frequency response is significant at higher frequencies (above $1kHz$) and it is incorporated in the CVT model. The TRANSFORMER model existing in EMTP has been used to represent the CVT step-down transformer with saturation.

STD Iron Loss Resistance also has considerable influence on frequency response and it should be included in the model.

Based on the above discussion, the CVT model for the DYNA-TEST Simulator has been simplified as shown in Figure 8.

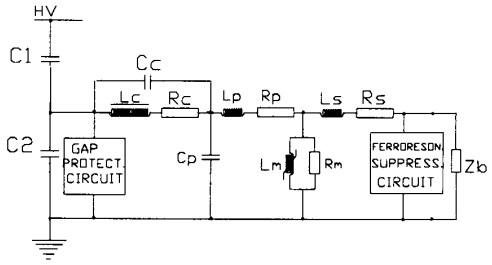

Figure 8. Simplified CVT Model Adopted for DYNA-TEST Simulator

Fault Simulation. The fault is simulated by an ordinary switch to ground in series with an impedance representing the fault impedance. It is critical to obtain the correct pre-fault conditions which will match with the pre-fault power flows in the system. This can be achieved by tuning the Thevenin voltage sources in the external system equivalent, so that the pre-fault currents injected by these sources into the study system match exactly with the pre-fault currents obtained from the full system's power flow results.

Simulation of transients produced during the circuit-breaker autoreclosing sequence can be accomplished by using the set-up given in Figure 9.

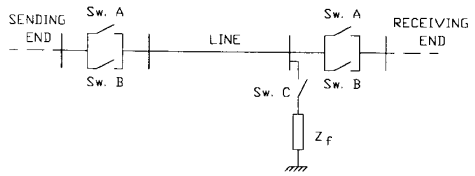

Figure 9. Autoreclosing Set-up

Three-phase high-speed autoreclosing sequence for a self-clearing phase- to-ground fault is simulated as described below. The voltage and current signals produced at the sending-end of the line are shown in Figure 10 and Figure 11 respectively.

Initially the system is in normal operating state and the circuit-breakers (switch A) at each end of the line are closed. Fault incidence is initiated at time t_F (9.4 ms) at the far end of the line by closing switch C. After a delay t_D (approx. 2.5 cycles) to account for the relay and breaker operation, the breaker poles (switch A) open at the current-zero after $t_F + t_D$ (55 ms) and isolate the faulted line. Reclosing is initiated after a dead-time t_R (approx. 6 cycles) during which the high-frquency transients are dissipated and new steady-state conditions are established. Also, this interval is sufficient for the fault-arc to extinguish; therefore, switch C is opened at time t_O (100 ms) to clear the fault. Autoreclosing of breakers is achieved by closing switch B at time $t_F + t_D + t_R$ (158 ms) and the system returns to the original state.

Recorded Data

The selection and use of actual fault data provided by the modern DFRs is by no means a straightforward task. Each record examination requires a knowledgeable operator. The operator should be familiar with the main sources of errors in these systems as well as with the DFR limitations.

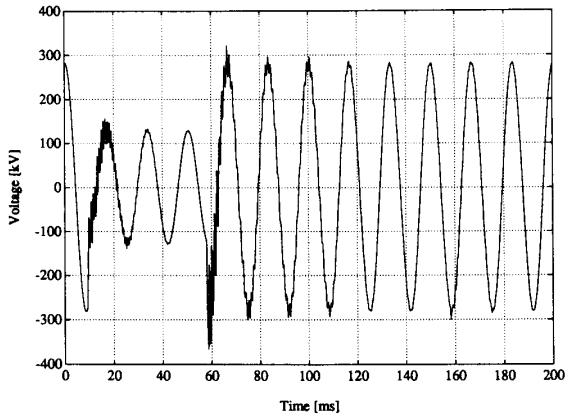

Figure 10. Faulted-phase Voltage

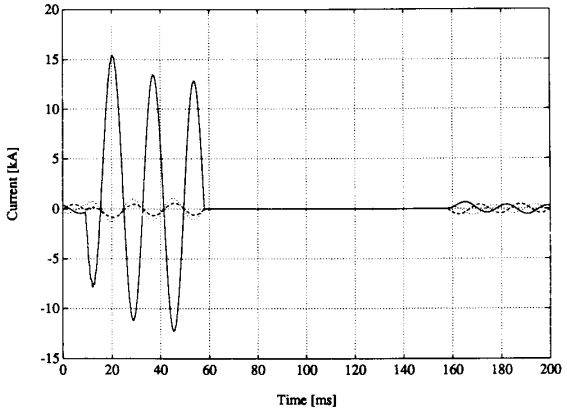

Figure 11. Line Currents

DFR processing errors. The main errors associated with digital data processing result from data sampling and finite A/D converter resolution.

Although the typical energy content of a power system transient falls off rapidly with increase in frequency, there is always a possibility that the fault signal will contain considerable high-frequency components. The finite sampling frequency used in DFRs imposes a limit on the highest frequency contained in the recording. Therefore, the use of anti-aliasing low pass filters in the DFRs becomes mandatory. The typical sampling rate of modern DFRs is between 3 and 12 kHz. It should be noted that DFRs providing multiple sampling rates should also have multiple/switchable low pass filters on all analog inputs. This is essential in order to avoid aliasing errors.

Another common error source is related to the A/D conversion resolution. Most of the available recorders use 12-bit converters. This is more than adequate for voltage transients, but might cause some unexpected problems when recording fault currents. Due to a high dynamic range of typical current signals, it is mostly guess-work and experience that determine the actual gain settings used on DFR inputs. A high gain may result in unwanted signal-clipping, while a low gain may result in a drastic reduction of the available resolution in the pre-fault portion of the waveform. This effect is illustrated in Figure 13, which is the enlarged portion of the pre-fault data taken from Figure 12.

In this case the gain scaling was close to optimum. It is visible that resolution in the prefault signals falls approximately to 5 bits. This is still sufficient for accurate estimation of pre-fault steady-state conditions, but leaves no head-room for gain setting errors.

All data files intended for dynamic relay testing should be checked for unwanted clipping with inappropriate files discarded from further use.

DFR limitations in pre-fault waveform generation. Depending on the relay design to be tested, the pre-fault portion of the waveform might have to be extended beyond the usual 2 to 3 cycles contained in the DFR data file. In this case the signal is extended by using the best fit sinusoids (one for each phase), synthesized from the previously identified steady-state parameters. Those parameters are:

- Recording System Offset
- Signal Amplitude
- Signal Frequency
- Phase Angle

Parameter identification is performed by means of non-linear four parameter curve-fitting, and requires that sufficient pre- and post-fault portions (2 to 3 cycles) are available in the reccord. The procedure is also sensitive to the recorded waveform resolution and might diverge due to incorect DFR gain settings affecting the pre-fault data resolution (current channels). It is important to note that the power frequency should not change significantly inside the steady-state interval used for parameter identification.

The curve-fitting process can be significantly simplified if the signal frequency is known precisely. However, this is usually impossible due to insufficient knowledge of the exact DFR sampling frequency used in the recording process.

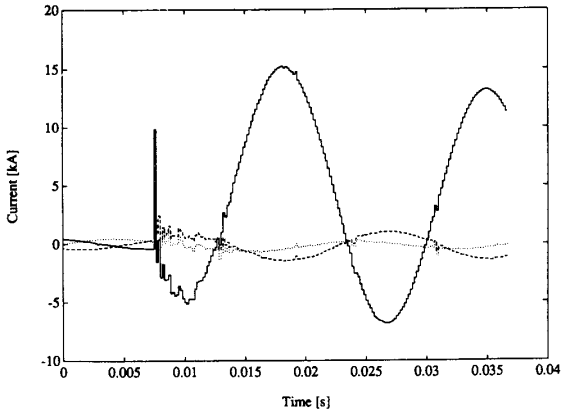

Figure 12. Current Transient Recorded During Typical Single Line to Ground Fault

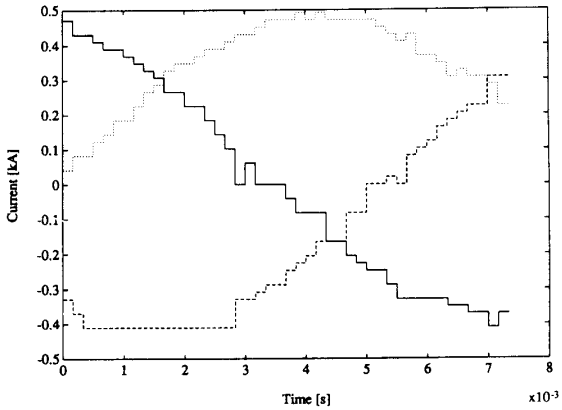

Figure 13. Pre-fault Portion of the Current Waveform

RELAY TESTING USING SIGNAL FILES

The actual relay testing on a DYNA-TEST Simulator consists of three distinct actions: test file preparation, test sequence execution, and test result analysis.

Test File Preparation

This activity is needed in order to convert the files coming from EMTPs and DFRs into the formats used by the test sequence execution and test result analysis software. All of the conversions provide the output in the quasi IEEE/COMTRADE format which was adopted as a central format for the DYNA-TEST Simulator system. This ASCII format was chosen for it's simplicity regardless of the file size drawbacks, which are partly alleviated in the conversion process by enabling the user to view and choose only the most interesting part of the waveform. It differs slightly from the proposed standard since only blank fields are used as data separators, omitting the commas proposed by the standard. This makes the files compatible with the MATLAB software package, although additional commas have to be inserted/deleted for data exchange with external users. This format coexists in parallel with the already mentioned LWB binary format used for D/A converter interfacing.

The use of ASCII data format greatly simplifies the EMTP file conversion. The conversion software first identifies the EMTP program version in order to acurately identify the exact starting point and format of the data fields. The user is then prompted with variable names in order to select the final output waveforms. All unnecessary data is then stripped off, leaving only the selected output channels. Finaly the blank spaces are inserted separating individual data values.

In our approach, the waveform reproduction system uses a fixed sampling frequency. Each input file with a different f_s must therefore pass through a sampling frequency conversion process prior to being allowed to proceed to actual waveform reproduction hardware. This is especialy important for DFR records whose sampling frequency is given by the actual DFR type and settings. The EMTP software on the other hand, already offers the possibility of arbitrary sampling frequency generation. The decimation option is also included in the package. Regarding the choice of sampling frequency for the EMTP output file, there are three possible options:

- Adjusting the simulation time-step to exactly match the reconstruction system sampling frequency.
- Choosing an integer multiple of the reconstruction system sampling frequency, and using the digital signal processing techniques to do the conversion.
- Choosing an integer multiple of the sampling frequency with the EMTP decimation option active.

It is only the first two options that give the correct result. The last option, although very simple should be avoided. Due to the possibility of aliasing, it does not always guarantee a correct result.

Direct generation of the required sampling frequency (first option), offers an elegant solution. The high frequency components will be slightly attenuated due to the nature of EMTP simulations (numeric integration), but the accuracy obtained is sufficient for most relaying studies.

The non-compromise approach calls for use of the sampling frequency conversion algorithm. In order to minimize the computation time spent in the conversion process, it is advisable to select the EMTP time-step in such a way as to produce the exact multiple of the waveform reconstruction system sampling frequency.

Since the DYNA-TEST Simulator operates with the waveform reproduction system sampling frequency fixed at 16 kHz, the recommended sampling frequencies for EMTP simulations are 32 or 48 kHz.

Test Sequence Execution

A typical test sequence consists of the following steps:

- Source file visualization and editing
- Frequency analysis and filtering
- Calculation of signal parameters

Source file visualization is performed by the MATLAB utility enabling easy signal displaying and editing.

Source file frequency analysis and filtering are needed when different relay algorithm features are to be evaluated. Analysis software capabilities are illustrated by comparison of the DFR recordings with EMTP simulation, given in the accompanying paper [29].

Calculation of signal parameters is also available for the purpose of more precise characterization of the relay test signals. Typical parameter calculations include: pre- and post-fault steady- state parameters, fault incidence angle, symmetrical components, power, frequency, and rms values.

Test sequence execution is related to the simultaneous generation of all the three voltages and currents by using the D/A converters. This may also include the contact signal generation.

Test Result Analysis

This step is the most important step in the overall relay testing since it is related to the final conclusion about the performance of a relay under test.

Signal processing features needed for this step are quite dependent on the specific tests and relays under consideration. Specific implementations of this step will be discussed in a future paper which will report results from some relay tests using the DYNA-TEST Simulator.

CONCLUSION

The discussion presented in this paper highlights the following DYNA-TEST Simulator features:

- It is a low cost, easy to implement relay test system.
- It is quite flexible in that it accommodates both field and laboratory test needs.
- It provides test signals that closely resemble the actual fault transients.

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