A DISTRIBUTED PROCESSING MICROPROCESSOR BASED HIERARCHICALLY STRUCTURED NETWORK (DMH) WITH APPLICATIONS TO THE CONTROL AND PROTECTION OF ELECTRIC POWER SYSTEMS

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ABSTRACT

Much good work has been done over the past decade on the development of digital computer based methods for the protection of electric power systems. The application of these Computer Relaying (CR) systems was not cost effective because the available computer equipment dictated a serial solution to what is in essence a parallel problem. The recent development of low cost, but very capable, microcomputers makes possible the consideration of a network of microcomputers as a cost effective way to implement CR systems. This paper considers the design of a Distributed Processing Microprocessor Based Hierarchically Structured (DMH) system for the protection of electric power systems. Some basic characteristics of the process of power system protection are analyzed. Considerations related to this new system concept are stated and the basic logical structure of the DMH system is described. Specifications are proposed for the necessary computer hardware, and a brief evaluation of available microcomputers relative to these specifications is given. Expected performance of the proposed DMH system is discussed and suggestions for further work are outlined.

I. INTRODUCTION

As the complexity and the level of transmission voltages of the power systems increase, the importance of the protection function within the overall functioning of the power system is increasingly becoming a popular issue. The cost of protection equipment is also an inseparable issue which comes into any considerations related to power system protection.

Reflecting all other relevant issues, the importance and the cost of the protection function have challenged the people at the utility companies, research institutions and universities to adopt the newest technologies and to develop improved methods and equipment for protection. CR is developing as a result of these efforts.

Specific performances of digital computers were recognized by researchers concerned with power protection applications sometime in the late 60's. Since that time, around 100 technical papers and publications [1,2,3] have been written on the subject and a number of research projects completed at the utility companies, research institutions and universities. Very few publications [4,5,6,7,8,9,10] have considered the applications of microprocessors to the CR field.

Our intentions in this paper are to induce a new concept that could be applied to form several protection functions within the power system, namely the DMH concept. In Section 2 some basic considerations of the protection task within the power system from the point of view of the DMH concept are analyzed. The basic logical characteristics of the DMH system are introduced in Section 3. In Section 4 specifications for system hardware are proposed and evaluation of available computer hardware relative to these specifications given. Section 5 gives some conclusions and some new ideas for further research activities.

II. SOME BASIC CONSIDERATIONS OF THE PROTECTION FUNCTION AS THEY ARE RELATED TO THE DMH CONCEPT

In this section the following protection systems will be considered:

- "classical" relaying systems (electromechanical and static relays)
- Computer Based Relaying (CBR) systems
- Microprocessor Based Relaying (MBR) systems

Terms CBR and MBR are introduced in this section in order to distinguish between two classes of computer systems used as protection systems: large computer systems (at least minicomputers) and microprocessor computer systems (microcomputers).

All three basic systems mentioned above will be compared and discussed through the discussion of several basic requirements of any system:

1. Utilization, or the percentage of time the system is efficiently used.
2. Accuracy, or ability to give an optimum response to a certain set of conditions.
3. Speed, or the ability to react quickly to a change in the inputs.
4. Flexibility, or the ability to adapt to functional changes.
5. Reliability, or the ability to provide predetermined changes in the outputs given a predetermined change in the inputs.
6. Security, or the ability to provide changes in the output conditions only when certain specified changes take place at the inputs.
7. Availability, or the ability to remain in the "ready to operate" mode.
8. Maintainability, or the ability to pass easily from a faulty state to a healthy state.

9. Simplicity, or the ability to perform the required functions with minimum hardware and minimum interaction between subsystems.

10. Low cost.

1. Utilization

It is a known fact that classical relays (electromechanical and static) are very poorly utilized devices. They are sitting on the lines "watching" for possible faulty conditions, in order to react. Of course, one can say that relays are utilized 100% since they are connected to the power systems all the time. But, if there is a way to perform the same functions of basic relaying and some other functions at the same time, then utilization of the classical relays is questionable.

CBR systems are devices which are in general intended to perform some functions besides the protection function. Nevertheless, since CBR systems are performing sequential operations as opposed to the parallel operation of analog relays, the calculation burden placed on digital computers is very heavy, and therefore the available time that could be devoted to some other functions would be very small.

MBR systems could introduce a parallel (non-sequential), distributed system and therefore the calculation throughput of the system would be pretty large which implies that there would be significant computational time available for some functions other than the protection function.

2. Accuracy

Classical relays are very much dependent on the "setting" conditions and the accuracy is highly dependent on fixed setting.

CBR systems are capable of performing calculations with very high accuracy, particularly in terms of error correction and estimation procedures. Accuracy of these devices is highly dependent on the algorithm used, and it can be significantly improved by better algorithms.

MBR systems are pretty much in the same range of accuracy as CBR systems speaking in terms of the characteristics mentioned.

Since the highest degree of information is contained in the shape of the signal waveform, and digital devices are capable of examining this shape, they are capable of performing high accuracy calculations. On the other hand, electromechanical relays are acting on the rms, static or the peak values and these values contain less information than the signal wave shape.

3. Speed

Classical relays have speeds that range from several cycles (electromechanical) to one cycle, and may operate as fast as 1/4 of a cycle (static relays).

Digital computers are capable of performing required calculations very fast, on the order of one cycle time or less, but since most of the algorithm requirements for high speed, the basi technological capabilities of digital computer are met pretty well with a processor having a instruction cycle time on the order of 1 μsec o less, a memory cycle time in the order of couple of hundred nanoseconds and A/D conversio times in the order of a couple of hundre seconds.

Microprocessor devices were claimed to b slower than digital computer devices, bu bipolar microprocessors can satisfy any of th functional speed requirements given above. O course, the bipolar devices are expensive, bu MOS devices with cycle times under 1 μsec ar also available today. DMH structure usin distributed processing algorithms (DPA's) woul provide concurrent processing which could in crease the speed of the required calculations.

4. Flexibility

Consideration of flexibility strongly favo digital systems because there is tremendou flexibility in the adjusting and changing o different features, doing that eithe automatically or at least with minor hardwar changes. A MBR system has some additional fea tures of modular expansion of the system's hard ware, as well as the system's software and firm ware. Special purpose hardware and programmabl memories are also available.

5. Reliability

Reliability of the classical relayin systems has been questioned. Some surveys [1 showed that within the protection equipment, th relays are the devices most likely to fail t operate, Particularly if they have not operate for a long time, their reliability is ques tionable.

Digital devices are very reliable device in general, and also have capability of self checking procedures.

CBR systems are very reliable, assumin reasonable software reliability, but some en vironmental conditions can significantly in fluence this reliability.

The MBR device is also very reliable but its distributed configuration might introduce some unreliable situations. But if we take into account reliability versus cost considerations, then we can conclude that if the device is chea then a high degree of redundancy, which can be considered as an improvement in reliability, might be very attractive. Reliability versus availability is also a central issue. Since the MBR device is flexible and allows easy replacement of faulty parts, the Mean Time Between Failures (MTBF) is of less concern than availability. Mean Time to Repair (MTTR) thus becomes a secondary issue if cheap and quick replacement of the erroneous devices can be performed. The relatively small size of the MBR system also allows the possibility of better protection of the system against environmental influences through appropriate shielding solutions.

6. Security

This issue is pretty much related to the reliability, availability and the maintainability issues. The particular feature of

The MBR system could be particularly attractive because of the possibility of implementing a modular security software which could be executed in a distributed fashion, concurrently in several locations.

7. Availability

In the section on reliability some relations between reliability and availability were emphasized. This relation should be particularly carefully studied as it is related to the DMH concept. Some of the features of interest would be the microprocessor back up devices capable of automatic replacement of the erroneous device as well as highly standardized plug-in microprocessor cards which could be exchanged very quickly.

8. Maintainability

It is probably evident that classical relaying devices require less time, skill and money to be repaired than digital devices.

Eventhough the digital devices are very reliable and therefore make the issue of maintainability less critical, it is still evident that very qualified personnel for maintenance purposes are needed.

Microprocessor based systems introduce some new aspects into the maintainability issue. The parts of the system that malfunction can easily, after replacement, be shipped to qualified and well equipped maintenance centers where quick and inexpensive maintenance can be performed. Eventhough the maintenance centers can be geographically separated from the installation location, the transportation facilities and low cost of transportation can still make maintainability highly efficient and considered together with availability and reliability highly flexible and economical.

9. Simplicity

It must be admitted that classical relaying equipment and configurations are, compared to the digital relaying systems, fairly simple, but the simplicity has to be in agreement with the level of complexity of the protection system used.

It is the authors' opinion that the DMH concept is logically simpler than any other digital relaying concept. Simplicity of the DMH concept is primarily due to its modular, distributed processing algorithm and its logical breakdown of the required functions by certain levels of functioning.

10. Low Cost

Cost is one of the major issues in the field of power system protection and is emplasized in this paper as one of the major issues of the DMH concept, too.

It is an evident fact that the cost of the classical relaying equipment and conventional digital computers have been substantially constant for a long time and do not show any significant trend towards going lower.

Microprocessor devices are showing a tremendous trend towards the lowering of its

It should be noted that these limits are ve
low and are coming near prices of $3.00 p
microprocessor chip in quantities and bel
$30.00 per microcomputer on a chip.

Of course the main cost reduction of t
DMH system would result from mass productio
but we are convinced that all other issues (1-
discussed above should be carefully studied a
utilized in order to favor the DMH concept
the less expensive way of protection.

As a conclusion to this section, it shou
be emphasized that digital protection syste
are surely more sophisticated systems than t
conventional relaying systems. This sophistica
tion should provide a more reliable, secur
better utilized, more flexible and accurat
protection system.

The other issues like maintainability
availability, cost, speed and simplicity are t
characteristics that should help distinguis
between the digital computer relaying concep
and the DMH concept.

In the following section some basic fea
tures of the DMH system are discussed and th
relation between these features emphasized.

III. THE DMH SYSTEM-ITS ALGORITHM AND ARCHITECTURE

In order to define the algorithm and th
architecture of the DHM system we will at firs
discuss the functional requirements of th
protection function as well as its logical deci-
sion structure. This will lead to the defini-
tion of the Distributed Processing Algorith
(DPA) and the Distributed Processing Architec-
ture (DPAR) of the DMH system. Normal and ab-
normal modes of operation of the DMH system are
also discussed. Specific characteristics of the
proposed DMH system are discussed at the end.

Functional Requirements and Logical Decision Structure

Protection of transmission lines, transformers, generators and bus bars as well as some other control and monitoring functions are assumed to be the set of protection functions which our system would handle.

Protection of each of the mentioned power system elements is a local function and can be performed almost entirely locally. The situations which introduce nonlocal requirements are special events, like very serious faults causing damage to the control equipment, etc. Delivery of the collected data, as well as certain backup situations are also nonlocal requirements. Of course, any change of the basic electrical characteristics of the power system being monitored would also require some communication facilities between the local protection systems.

Local protection function can be fairly complex, consisting of several decision functions. Data obtained by sensors could be shared between these decision functions. Therefore, some coordinating function should be performed at the local protection systems.

While performing certain protection functions, the local protection system is actually converting the local data collected by sensors into new data base. This can be viewed as a preprocessing function, preparing data for some

quires data fron other local systems and/or from the central control system. Therefore a connecting function providing a connection between the local systems and other related systems should also be provided.

It becomes evident that there should exist a point where the concentrating function could be performed. This function will mainly allow the concentration of data preprocessed at local points in order that the concentrating system can analyze the data, as well as make relevant decisions and send them to the local point and elsewhere.

We are assuming that there exists an overall protection function within the power system and therefore some central decision function also exists but, as far as the proposed DMH system is concerned, the problem of the central decision function is beyond the scope of this paper.

DPA and DPAR of the Proposed DMH System

From the discussion given above we can define the following DPA's:

1. There is a set of different algorithms performed by local points. Local point algorithms can be performed concurrently.

2. There is a set of coordinating algorithms for each particular protection function which coordinate execution of the local point algorithms.

3. Separate algorithms are necessary to handle communications between the local points and the concentrating point. These algorithms are logically dependent and are executed in some arbitrary order.

4. A set of algorithms is necessary to coordinate the execution of the algorithms given above (1, 2, 3). Since algorithms 1, 2, and 3 can be performed concurrently, the algorithms of the concentrating point should coordinate possible interactions between algorithms 1, 2 and 3.

5. There exists a distributed data base which is preprocessed by algorithms 1, 2 and 3 respectively, and made available to algorithm 4. The data base at each stage of transformation is stored and maintained as a local data base and is unchanged until the moment when the distributed data base is updated as a whole. There exists a set of algorithms which takes care of the described operations that are performed on the distributed data base.

DPAR characteristics are:

1. There are 4 levels in the hierarchy where the following units are located:

   -Local processing units (level 1)
   -Coordinating units (level 2)
   -Connecting units (level 3)
   -Concentrating units (level 4)

2. Levels 1, 2 and 3 represent the major part of the DMH system. Level 4 is intended for minicomputer applications could be implemented using microprocessors.

3. The proposed DMH system consisting o levels 1, 2 and 3 is intended for single substation application wher level 4 would be monitored by miniconputer. This situation determines the number of units at each leve of the DMH system.

4. Each level has its own memory storag and it is connected to the common bu of that level.

5. The flow of information data in th structure is mostly from local point up to the concentrating point. Th flow of control data is mostly from th concentrating point down to the local points but in both the mentioned case there is a possibility of reverse flo of the information and control data.

6. Interrupts are issued ordinarily in th direction from level 4 towards level 1 but, on some rare occasions the othe direction is also possible but in a stepped fashion from level to level.

7. Ordinary, polling and scanning capabilities are used for normal reporting procedures established between levels 1, 2, 3 and level 4.

Proposed DMH System

The proposed system is represented in Figure 1. The configuration given in Figure 1 operates in two basic modes:

-The normal mode of operation
-The abnormal mode of operation

The normal mode of operation assumes, basically, the concurrent operation of local systems with an established procedure for reporting the status data to the concentrating system. The system can be viewed as a transformation system which takes data from the system at level 0 (senors), preprocesses that data, makes some decisions and sends the data to the upper levels. So there exists a transformation and updating of local data bases, while the flow of information is from lower levels to the upper levels. There is an established order as to how the concentrating system takes data from the lower levels, makes decisions and sends back the control data.

The abnormal mode of operation changes, in a sense, the operational characteristics of the system given above. In an abnormal situation one of the local systems detects the abnormality and reports that immediately to the upper levels.

Depending upon the importance and complexity of the abnormal situation, help might be requested through all of the levels up to the concentrating system. In this case, all other local point systems would perform almost totally independent operations, allowing the concentrating system to be devoted to the local point system where the abnormality has occurred. These "independent" local point systems should also be ready to respond to possible unusual requests for information and control data. After the abnormal situation vanishes the restorative mode of operation should establish all the conditions required for the normal mode of opera-

Characteristics of the Proposed DMH System

All of the parameters discussed in Section 2 could now be discussed in more detail. However, we will assume that it will be more interesting to summarize some important features of the DMH system which would involve several of the parameters given is Section 2 at the time.

These features are:

1. The DMH system can be developed as a general system which could be applied to most of the protection environments.

2. Hardware structure could be made fully programmable allowing for specific characteristics to be incorporated in the general system.

3. Hardwired communications protocol should be flexible enough to allow fully expandable and flexible microprocessor networks.

4. Hierarchical architecture of the microprocessor network provides an optimal throughput of the data and control messages, and is fully suitable for the logical requirements of the protection function. Deadlock situations are highly unlikely for the given flow of interrupts.

5. Redundant memory configuration at each level enables a store-and-forward way of transmitting data from local data bases to the central data base. It also allows a data block transfer without placing a great data flow burden on common buses at each level.

6. Redundant hierarchical configuration was not particularly discussed, but the standardized network as it is described would allow attachment of any number of redundant pieces of hardware without any particular problems.

Having defined the proposed DMH system, we now proceed to develop specifications for the necessary hardware and software, and to provide a preliminary evaluation of available off the shelf products for this application.

IV. EVALUATION OF AVAILABLE MICROCOMPUTER HARDWARE FOR PROPOSED MDH SYSTEM

This section considers the capability of available hardware relative to the requirements for components of the DMH system as discussed in Sections 2 and 3. The discussion is divided into consideration of the following subsystems: memory, communications, Input/Output, and the central processors. Two approaches to implementing the DMH system are discussed briefly: the first optimizes the choice of hardware for each of the functions at the integrated circuit chip level, and requires the design of the microcomputer subsystems; the second approach optimizes the choice at the level of available microcomputer systems.

Memory Subsystems

Memory devices are available today in a wide variety of sizes and technologies such as: 8K, bipolar PROM; 16K, bipolar ROM; MOS EPROM from 16K to 64K; bipolar RAM from 1K to 16K; up

nology. The manufacture and sales of memor devices is highly competitive with a lar number of manufacturers participating in thi market. All important products are secor sourced. It is our opinion that the necessa memory components with adequate capacity ar speed can be selected from off the shelf, star dard products, which have demonstrate reliability.

Communications Subsystems

Prior to several years ago, the design of communications interface for use in compute networking was a major project involving sub stantial time and money. Many of the standar communication functions are now available in on to a few integrated circuit packages such a UART's and USART's. It is our opinion that suc packages together with a simple microcompute can solve the intercomputer communication problems to be encountered in the implementatic of a DMH system in a cost effective manner.

Input/Output Subsystems

Integrated circuit packages have bee developed to perform many of the elementar functions of moving information into and out o the functional blocks of computer systems. Th proposed DMH system requires I/O interface to variety of devices such as: memory, regular an DMA; interrupt handling; data acquisition sub systems; special processors such as digita filters. It is again our opinion that availabl integrated circuit packages together with simpl microcomputers can be assembled to provide cos effective programmable I/O subsystems. This ap proach to the design of this computer network i consistent with the design philosophy used fo the design of large scale computer systems fo the last decade. Again, it is the advent o medium and large scale integration in th manufacture of integrated circuits and microcom puters which makes it possible to apply this ap proach to the design of systems such as th proposed DMH.

Central Processor Subsystems

The phrase Central Processor may call to mind the central unit of a large scale computing system. However, the term is used here to identify the units responsible for processing the algorithms used to identify and evaluate the nature of the fault or other abnormality on the electric power system. The following characteristics of microprocessors are important relative to the DMH application:

* Direct Memory Access (DMA)
* Word Length (WL)
* Instruction Cycle Time (ICT)
* Programming Language Options (PLO)
* Chip Technology (CT)
* Interrupt Capabilities (IC)
* Second Source Availability (SSA)
* Number of Instructions (NI)
* Microprogramming Option (MO)

The table shown in Figure 2 summarizes the characteristics of currently available microprocessors which might be considered for the implementation of a DMH prototype system. Although it would be convenient from a compatibility point of view, both hardware and software, to select one type microprocessor for all units in the DMH system, it is probable that

MANUFACTURER	MODEL	CT	SSA	WL bits	CF MHz	NPPC	NI	DMA	IC	PLC	MO
ADV.MIC.DEV.	AM9080A	NMOS	INTEL,NEC	8	4	2	78	YES	YES	ASMB,HL	NO
FAIRCHILD	F8	NMOS	MOSTEK	8	2	1	70	OPT	YES	ASMB,HL	NO
HUGHES AIRC.	HCMP/ 1802CD	CMOS	RCA	8	6.4	1	91	YES	YES	ASMB	NO
INTEL	8080A2	NMOS	TI,AMD	8	2	2	78	YES	YES	ASMB,HL	NO
INTEL	8085	NMOS		8	3	1	80	YES	YES	ASMB,HL	NO
INTEL	8748/ 8048	NMOS	AMD	8	6	-	90	NO	YES	ASMB	NO
MOTOROLA	6800	NMOS	AMD,HIT.,FC	8	1	2	72	OPT	YES	ASMB,HL	NO
NEC	μPD8080A	NMOS	AMD,INTEL,TI	8	3	2	78	YES	YES	ASMB,HL	NO
SIGNETICS	8X300	BiP	SMS	8	4	4	8classes	NO	NO	----	--
ZILOG	Z80	NMOS	MOSTEK	8	4	1	158	YES	YES	ASMB,HL	NO
HARRIS SEMI.	HM6100A	CMOS	INTERSIL	12	8	10	70	YES	YES	ASMB,HL	NO
PANAFACOM	L-16	NMOS		16	2	2	33	YES	YES	ASMB	NO
TEXAS INST.	TMS9900	NMOS		16	3	4	69	YES	YES	ASMB,HL	**
TEXAS INST.	SBP9900	IIL		16	3	1	69	YES	YES	ASMB,HL	**
ADV.MIC.DEV.	AM2901A	RAYT.,MOT.		4bS*	8	1	var	OPT	OPT	MICROPROG.	YES
MONOL.MEM.	6701	BiPS**		4bS	10	10	36	--	--	----	--
MOTOROLA	2900	LSTTL	AMD,RAYT	4bS	9.5	var	unlim	OPT	YES	MICROPROG.	YES
MOTOROLA	10800	ECL		4bS	12.5	var	unlim	OPT	YES	----	--
SIGNETICS	3002	BiPS	INTEL	2bS	7	1	40	OPT	OPT	MICROPROG.	YES
TEXAS INST.	SBP/0400	IIL		4bS	4	1	512	YES	YES	MICROPROG.	YES
TEXAS INST.	74S481	BiP		4bS	10	1	512	YES	YES	----	--

*4bS- 4 bit slice; **BIPS- Bi-polar Schotky

FIGURE 2: TABULATION OF CHARACTERISTICS OF SELECTED MICROPROCESSORS AVAILABLE MAY 1978

required in the central processing type functions will require a 16 bit word to provide adequate precision in the arithmetic operation. The use of double precision arithmetic routines would probably limit the utility of the 8-bit processors for this application. On the other hand, it seems likely that the 8-bit processors may prove to be adequate and cost effective in the role of programmed controllers for I/O and communications functions. Special processor type chips have recently become available which are designed to perform floating point arithmetic as a hardware function, rather than programming such operations in software. Packages are also available to implement hardware subroutines to calculate trignometric and logrithmic functions. These special packages can be utilized if it is necessary to speed up the arithmetic in order to complete the fault analysis algorithms in desired time period.

The table provides a comparison of two different parameters which are related to the speed at which the processor can execute programs. The first is the basic clock frequency (CF) and the second the number of phases per cycle NPPC. It is our opinion that microprocessors can be chosen from those available which will be cost effective for the implementation of a prototype DMH system.

One approach would be to select the microprocessor chip which is optimum for each module of the systen and design that module as a special purpose microcomputer system. The second is to select appropriate microcomputers as provided by a number of vendors, and develop only the interface circuitry to create the protype modules for the DMH system. Examples of microcomputer boards which are available and candidates for consideration are: INTEL SBC 80/20-4; Data General, micro-NOVA; Digital Equipment Corporation, LSI-11 series; MOSTEK, Z-80 OEM controller; Texas Instruments, 990/4; and MOTOROLA MEC 6800B. We believe that the second approach would be the most cost effective way to create prototype DMH system for evaluation and field testing. At the time such a system was to be produced and installed in quantity, the first approach would likely produce the most cost effective system.

V. CONCLUSION

As a conclusion to our discussion we want to emphasize the following, in our opinion interesting, points discussed throughout the paper:

1. The main characteristics of the research performed in the field of CR so far is primarily based on single, large scale computer systems (at least a minicomputer) and algorithms are not classified as DPA's.

2. The introduction of LSI technologies in the early 70's have given some new possibilities to the consideration of the CR as a whole.

3. The DMH concept is a logical and feasible possibility for the implementation of LSI to the CR problem.

4. DPA's, functionally divided "vertically" and "horizontally", as well as the DPAR of the proposed DMH system, are very suitable for actual protection systen requirements.

5. The hardware needed to implement the proposed network of microprocessors is available as off the shelf components today.

This paper evolved from some analysis and studies of the CR field performed in our department. We are currently in the stage of specifying the design requirements for DPA's and DPAR for the protection of the different elements of the power systems. Some design activities for the overall protection system based on the DMH concept have already been performed and we are looking forward to publishing the results in a future paper.

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MAY 1978

MANUFACTURER	MODEL	CT	SSA	WL bits	CF MHz	NPPC	NI	DMA	IC	PLC	MO
ADV.MIC.DEV.	AM9080A	NMOS	INTEL,NEC	8	4	2	78	YES	YES	ASMB,HL	NO
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TEXAS INST.	3BP9900	IIL		16	3	1	69	YES	YES	ASMB,HL	?
ADV.MIC.DEV.	AM2901A	RAYT.,MOT.		4bS*	8	1	var	OPT	OPT	MICROPROG.	YES
MONOL.MEM.	6701	BiPS**		4bS	10	10	36	--	--	----	--
MOTOROLA	2900	LSTTL	AMD,RAYT	4bS	9.5	var	unlim	OPT	YES	MICROPROG.	YES
MOTOROLA	10800	ECL		4bS	12.5	var	unlim	OPT	YES	----	--
SIGNETICS	3002	BiPS	INTEL	2bS	7	1	40	OPT	OPT	MICROPROG.	YES
TEXAS INST.	SBP/0400	IIL		4bS	4	1	512	YES	YES	MICROPROG.	YES
TEXAS INST.	743481	BiP		4bS	10	1	512	YES	YES	----	--

*4bS- 4 bit slice; **BiPS- Bi-polar Schotky

FIGURE 3: TABULATION OF CHARACTERISTICS OF SELECTED MICROPROCESSORS AVAILABLE MAY 1978

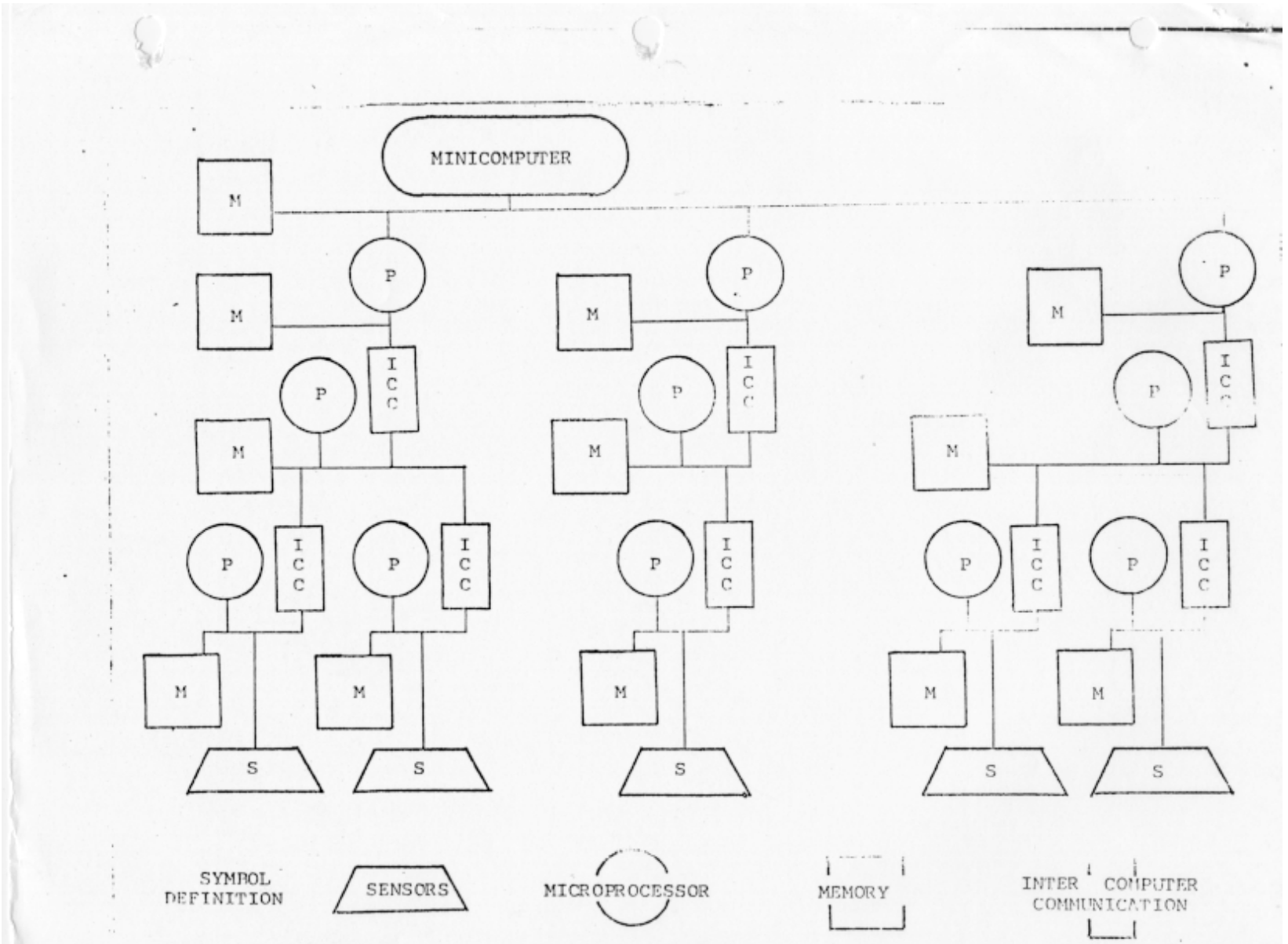

FIGURE 1: BLOCK DIAGRAM OF A DISTRIBUTED PROCESSING MICROPROCESSOR BASED HIERARCHICALLY