IMPLEMENTATION OF A DISTRIBUTED DIGITAL BUS PROTECTION SYSTEM

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Abstract: A new distributed principle of bus protection is presented. The protection system description, its design features, hardware structure, data communication network construction and protection algorithms are discussed. Performance analysis and preliminary experiments show its distinguishing advantages over the traditional centralized principle.

Keywords: Bus Protection, Data Communication, Digital Relaying

INTRODUCTION

Rapid development of power systems and an increase of their capacity require highly reliable protective relaying principles and devices for their high voltage bus – the energy concentration and distribution point. For the traditional principle of bus protection, it is necessary to lead the secondary currents of all the CTs to a central differential relay, which calculates the differential and the restraint current, compares them and makes the decision whether to trip all the circuit breakers connected to the bus. If the differential relay trips all the circuit breakers connected to the bus during external faults, or misoperates in normal operating conditions, due to incorrect settings, electromagnetic interference or component failure, this will cause serious consequences for the power system.

The improvements in the reliability of the bus protection operation can be achieved by exploring two options. One is to strive for more selective or dependable centralized solution by improving the measurement and computation using digital technology [1]. The other option is to implement a new distributed principle of the bus protection by exploring the capability of the new communication technology becoming available in the substations [2].

The utilization of the new communication technology is quite appropriate since extensive research and development activities are being pursued in this area today [3].

This paper concentrates on an option of developing a new bus protection principle based on a distributed, rather than centralized, algorithm processing principle. The first part of the paper discusses the basic principle of the distributed bus protection. The next three sections give implementation details regarding hardware, communications, and algorithms. The test results and conclusions are given at the end.

PE-318-PWRD-0-12-1997 A paper recommended and approved by the IEEE Power System Relaying Committee of the IEEE Power Engineering Society for publication in the IEEE Transactions on Power Delivery. Manuscript submitted July 25, 1996; made available for printing December 17, 1996.

THE DISTRIBUTED BUS PROTECTION PRINCIPLE

In order to eliminate the inherent weakness of the traditional centralized principle of bus protection, this paper uses a new distributed bus protection principle by which the whole bus protection system is divided into a number of protection units, each installed on one circuit of the bus (incoming or outgoing transmission line or transformer). All these protection units are connected by a data communication network. Each of the units carries out sampling and A/D conversions of the current waveform samples of its own circuit and sends them out through the communication network to all the other protection units. It also sends out the information about the operating status of this circuit, such as to which section of the bus system it is connected.

To realize the differential bus protection with a percentage bias restraint characteristic, every protection unit, having received samples of the currents and contacts' status of all the circuits connected to the bus, will be able to carry out the computation and comparison of the differential and restraint currents and make the decision whether or not to trip its own circuit breaker. If a fault happens on the protected bus section, all the protection units of this bus section will trip their own circuit breaker and clear the fault. If one of the protection units misoperates in the normal conditions owing to the electromagnetic interference, or component failure, etc., it may trip only its own circuit breaker, not affecting seriously the power system operation. In addition, this misoperation may be verified by the information about the behavior of other protection units, and then corrected by automatic reclosing of the wrongly tripped circuit breaker.

The distinguishing features of this new principle are summarized below:

- The most serious catastrophe of the whole bus blackout due to maloperation of bus protection will be avoided.
- The current ratios of the CTs do not necessarily have to be equal and the auxiliary CTs are not necessary.
- The wiring of the secondary CT circuits will be greatly reduced and simplified. The bus protection units of every line may be installed on the same panel together with the line protection and share the CT secondary cable. It is not necessary to lead the CT secondary cables of all circuits to a central bus protection panel.
- These bus protection units, using a powerful microprocessor, may easily combine in itself another duplicate main protection of the transmission line, or trans-

former, and serve as their backup protection, improving the protection reliability. At the same time, the line and the transformer protections can easily serve as the backup of the distributed bus protection.

- This protection has capability of automatic adaptability to the change in the operating modes of the bus system.
- The data communication network can be connected with the computer network of the substation, and even the whole power systems. Thus, the bus protection devices can share and receive the substation and system data which provides the possibility to further enhance the adaptability of the overall system protection.

HARDWARE ARCHITECTURE

1. Bus Protection System

Figure 1 shows the basic architecture of the distributed bus protection system. The protection units installed (each on one connected circuit of the bus system) and the monitoring unit, are connected by the data communication network. The bus system of the substation may have any configuration such as single bus with a sectionalizing circuit breaker, double bus with connecting circuit breaker, double bus with $1\frac{1}{2}$ circuit breaker scheme, etc. The protection unit carries out data acquisition on the circuit on which it is installed, transmits it to the other protection units, receives data from other units, calculates currents and voltages for differential protection, locates fault position and makes the tripping decisions. The voltage data is used to realize the auxiliary under voltage fault detection to increase reliability. The monitoring unit synchronizes the sampling clock of all the protection units. The synchronization may be conducted once per second. The protection units stop receiving the synchronizing signal during fault conditions so that the possible failure of the monitoring unit does not affect the operation of the protection units during faults. The monitoring unit also supervises continuously all the protection units during normal operating conditions. The current tendency concerning synchronization is to build up a central synchronizing clock in the substation implemented with global positioning system (GPS), which is responsible for synchronization of the microprocessor based protection and control devices. If this will be done, the monitoring unit may not be necessary.

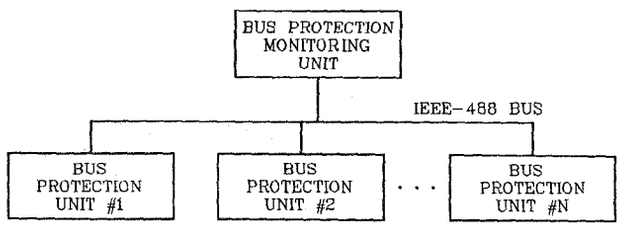

Fig. 1. Architecture of the Distributed Bus Protection System

2. Construction of the Protection Unit

The protection units are three-processor devices; their schematic diagram is shown in Figure 2. CPU1, a single chip processor Intel 8797BH, is responsible for data acquisition. It takes sampling and executes A/D conversion of the three phase and zero sequence voltage and current samples of the circuit on which it is installed. It also collects the information about the connection status of this circuit (the bus section it is connected to) and position of its circuit breaker (closed or open). It writes this data to the shared and dual port RAM for communication with CPU2 and CPU3. CPU2 is also a single chip processor Intel 8097BH; it works as a communication processor. It reads from the shared RAM the current data and transmits it to the other protection units through the IEEE-488 bus. It also receives the current data from all the other protection units and writes it to the shared RAM.

The CPU3 is a single chip microprocessor TMS320C30 serving as a protection processor. In every sampling period, the data acquisition CPU1 reads from shared RAM the samples of currents and associate status information and rewrites them to the dual port RAM, so that all the data necessary for calculating the differential and restraint currents are stored in the dual port RAM. The protection CPU3 uses this data for realization of the bus differential protection.

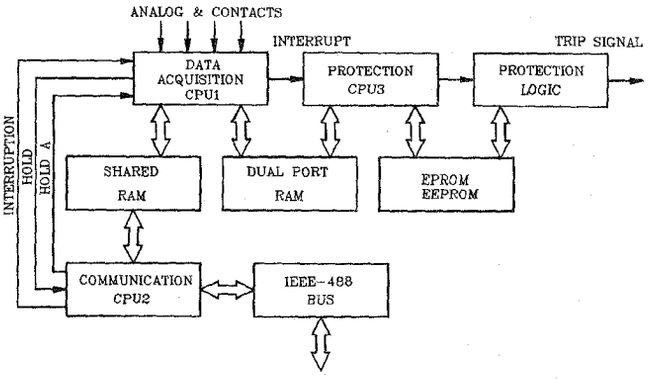

Fig. 2. Multi-Processor Architecture of the Bus Protection Unit

DATA COMMUNICATION NETWORK

1. Application Requirements

The data communication network requirements of the proposed distributed bus protection are simplicity, reliability and sufficient speed of data transmission. The required speed of data transmission may be evaluated by the following example [2].

Assume the sampling frequency is taken as 1000 Hz, i.e., time interval between two samples for the 50 Hz system is 1 ms. Take the number of circuits connected to the bus to be 14.

The waveform samples and status information to be transmitted from every protection unit are (see Fig. 3):

1) Zero sequence and the three phase currents (each of them takes 16 bits) which amounts to 64 bits
2) Cyclic redundancy code has 16 bits (one "packing" and fifteen code bits) which makes 75 bits of code and 5 packing bits
3) Status information about the number of bus sections to which the given circuit is connected and the position of its circuit breaker, have 8 bits each which amounts to 16 bits
4) 8 bits opening flag, 8 bits address code (number of the

circuit on which the given protection unit is installed), 16 bits time code, 8 bits closing flag. These additional transmitting codes amount to 40 bits.

All the above data constitutes a 200 bit "data message," which should be transmitted in every sampling interval, as shown in Figure 3. Therefore, in the case with 14 circuits, the whole message which should be transmitted and received in 1 ms will be 2,800 bits long. It means that the minimum speed of data transmission required is 2.80 Mbps.

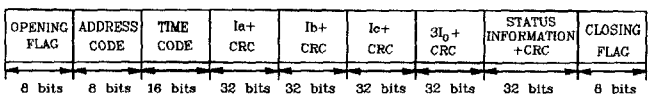

Fig. 3. Pattern of the Data Message

The communication may be conducted using a version of the token bus protocol in the following way. At the beginning of every sampling period, the protection unit Number 1 sends its data to all other units. After completing its sending, the protection unit Number 1 passes the token to unit Number 2, and then unit Number 2 begins to send out its data. After completing its sending, the token is passed to unit Number 3, and so forth. At the next sampling period after the new data is collected, the new round of data transmitting and receiving starts. At the same time, the protection unit CPU3 proceeds with error detection, correction, and bad data elimination and executes the protection programs by using every new data set.

2. Application of the IEEE–488 Bus

The IEEE–488 standard bus [4] can meet the above demands. It uses the 8 bits by parallel and every byte by serial transmitting mode. According to the standard worked out in 1978, the speed of data transmission reaches 8 Mbps. It permits many different devices to have the same address, i.e., to realize data communication by broadcasting mode. It is designed to provide a common communication interface among devices over a maximum distance of 20 meters at a maximum speed of 8 Mbps. Up to 15 devices may be connected together [4,5]. But if the GPIB–130 type extender is used, the maximum cable distance may be extended to 300m, and the number of devices may be expanded to 28.

It is composed of eight data lines, five interface management lines and three handshake lines. By using the above 16 lines, the IEEE–488 also provides 11 interface functions, 5 universal commands, 5 address commands which make this interface bus system suitable for many applications.

As mentioned above, the bus protective relaying system demands maximum simplicity and the greatest reliability. As the data to be transferred and the transmission process for the bus protection have definite specifications and strict regularity, not all of the above functions and commands are necessary for this purpose. The main control functions and interlocking procedure used, as well as the data transmission implemented, may be explained as follows.

The **control function** transfer should be conducted by the following procedure. At first, the present controller–in–charge (for example protection unit Number 1) drives the "Attention" (ATN) signal to low, and then sends the "Talk Address" of the new controller–in–charge (protection unit Number 2) by 8 data lines, and at last, sends the command "Take Control" (TCT). By receiving from the bus, its own talk address and the command TCT, the new controller–in–charge (i.e., the protection unit Number 2) begins to deliver its current data from the circuit on which it is installed. After completing data transmission, the protection unit Number 2 transfers the control function (passes the token) to the protection unit Number 3. Thus, the controller–in–charge will be transferred in this manner from the first unit to the last unit, and then returned to the first one when a new round of data transmission starts.

For every data transmission, the three line **interlocking (handshake) procedure** is necessary to ensure the reliability and correctness of transmission.

Refer to the logic diagrams in Figure 4. The bus voltage level is said to be high when voltage is $\geq 2V$ and is low when voltage is $\leq 0.8V$, thus:

Bus DAV="low" means that the data on the 8 data lines are valid.

Bus NRFD="low" means that not all of the listeners are ready to accept data.

Bus NDAC="low" means that not all listeners have read the data on the bus yet.

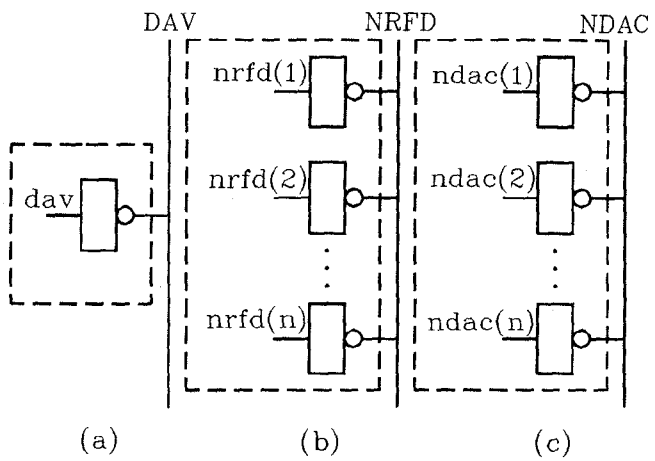

Fig. 4. DAV, NRFD, NDAC Message Logic

Note: dav, nrfd, ndac represent the device functions inside the device. DAV, NRFD, NDAC represent the bus functions of the IEEE–488 bus.

For example, a protection unit, the talker, is ready to start a data transfer to all the other protection units. At the beginning of the handshake, NRFD is high indicating that all the listeners are ready for data receiving. The NDAC is low, indicating that the listeners have not accepted the data since no data has been sent yet. The talker places data on the data lines, waiting for the required settling time, and then indicates valid data by driving DAV to low. All listeners drive NRFD to low indicating that they are not ready for more data. They then read the data and drive NDAC to high, indicating acceptance. The talker responds by resetting DAV and prepares itself to transfer the next byte. The listeners respond to DAV high by driving NDAC to low. The talker can drive the data lines with a new data byte and wait for NRFD to be high to start the next handshake cycle.

3. Error Control

The error control coding technique is an important and effective measure to eliminate the data transmission error and ensure the correctness of relay operation. Here, we use one of the best multiple-error–correcting codes, the Bose–Chaudhuri–Hocquenghem (BCH) codes [6]. They are linear block codes (n, k), where $n = 31$ is the length of the codes, $k = 16$ is the length of the data to be transferred. It possesses the ability to detect and correct 3 or less errors in the accepted data, i.e., $t = 3$. The generator polynomial used is:

$$g(x) = x^{15} + x^{11} + x^{10} + x^9 + x^8 + x^7 + x^5 + x^3 + x^2 + x + 1 \quad (1)$$

If the information to be transmitted, and the checking numbers are expressed as polynomials $m(x)$ and $r(x)$:

$$m(x) = m_{k-1}x^{k-1} + m_{k-2}x^{k-2} + \ldots + m_0 \quad (2)$$

$$r(x) = r_{r-1}x^{r-1} + r_{r-2}x^{r-2} + \ldots + r_0, r = n - k \quad (3)$$

then, the code transmitted by the communication channel, expressed also as a polynomial, is:

$$C(x) = C_{n-1}x^{n-1} + C_{n-2}x^{n-2} + \ldots + C_0 = x^{n-k}m(x) + r(x) \quad (4)$$

The encoding and decoding methods of this code are similar to that for other cyclic codes.

Encoding a BCH code may be realized by multiplication of the information polynomial $m(x)$ by x^{n-k} and then dividing $(mod\ g(x))$ by $g(x)$ to get the remainder polynomial $r(x)$. The latter is the checking polynomial. That is:

$$\frac{x^{n-k}m(x)}{g(x)} = q(x) + \frac{r(x)}{g(x)} \quad (5)$$

$$x^{n-k}m(x) = q(x)g(x) + r(x) \quad (6)$$

or

$$r(x) = x^{n-k}m(x) \quad (mod\ g(x)) \quad (7)$$

The encoding procedure may be realized by a shift register encoder or by a computer program. In this paper, the latter is adopted.

The following is a description of the **decoding method**. Assume that there are v errors occurring at bits i_1, i_2, ... i_v, then the error pattern $E(x)$ is:

$$E(x) = e_{i_1}x^{i_1} + e_{i_2}x^{i_2} + \ldots + e_{i_v}x^{i_v} \quad (8)$$

Let us assume the actual transmitted polynomial is $C(x)$. Let H represent the checking matrix of these BCH codes; we have:

$$CH^T = 0 \quad (10)$$

then :

$$R(x)H^T = C(x)H^T + E(x)H^T = EH^T \quad (11)$$

To calculate the syndrome S from R and H:

$$S = RH^T = EH^T \quad (12)$$

If $S = 0$, it means $E = 0$, i.e., no error is contained in the received polynomial $R(x)$. The errors or error exist(s) if S is not equal to zero. Therefore, the decoding operation consists of calculating the syndrome.

The syndrome calculations of such good codes with better error controlling property are generally very complicated, and thus, it becomes important to reduce the complexity of the calculation algorithm. Here, we use the Winogard algorithm for fast convolution [6]. It breaks a convolution into a number of short convolutions that are easy to compute. The short convolutions are then recombined using the Chinese remainder theorem [6] for polynomials. This method reduces the number of multiplications and additions in computation, and therefore, reduces the time of decoding.

PROTECTION ALGORITHMS

Bus protection should operate as quickly as possible. The best approach is to compare instantaneous values of the currents before saturation of the current transformers. After saturation, the instantaneous values are severely distorted. In that case, the phasors (not instantaneous values) of the currents should be calculated and compared.

In this paper, the following combination of steps is proposed. Within t_s (time t_s before the CT saturation is taken as $\frac{1}{4}$ period in this paper) from fault occurrence, both instantaneous values and phasors of the currents are calculated. However, only the instantaneous values are used to decide the response of the relay according to formula (13). After $\frac{1}{4}$ period, calculation of the instantaneous values is stopped. The calculation of current phasors is continued.

1. Criteria for Relay Operation

A. Criterion of Operation before CT Saturation

The following criterion is used:

$$\sum_{m=1}^{M} \Delta i_{m,k} \geq i_0 \quad (13)$$

Where $\Delta i_{m,k} = i_{m,k} - i_{m,k-N}$ is the variation of the fault currents in the first period after the fault. M is the number of circuits connected to the protected bus section. N is the number of samples in one cycle. $i_{m,k-N}$ is the current of the m-th circuit one cycle before with respect to the sampling point k. All the variations are caused by the same fault and are nearly in phase. i_0 is the setting value determined by the sum of the maximum errors of unsaturated CTs, as well as the error in data processing plus the necessary margin. If (13) is fulfilled 4 times out of 5 consecutive calculations, the relay operates and trips the related circuit breakers. For $N = 20$, the relay may operate within 5ms for 50 Hz power system.

B. Criterion of Operation after t_s

The following criterion is used:

$$|I_1 + I_2 + \ldots I_M| - K\{|I_1| + |I_2| + \ldots |I_M| - I_d\}^+ \geq I_0 \quad (14)$$

where $I_1, I_2, \ldots I_M$ are the current phasors of the M circuits connected to the bus to be protected (positive direction of the currents is taken as towards the bus), K is the restraint factor; $\{\ \}^+$ means that it gives the contribution only when the value in $\{\ \}$ is positive. I_d is a setting value determining the intersection point of the restraint characteristic.

In the case of an external fault on the circuit M, all the currents, except I_M, are in phase. Since I_M is opposite

in phase equation (14) becomes:

$$|I_1 + I_2 + \ldots - I_M| - K\{[I_1 + I_2 + \ldots + I_M] - I_d\}^+ \geq I_0$$

Let $I_N = I_1 + I_2 + \ldots + I_{M-1}$. Then:

$$|I_N - I_M| - K\{[I_N + I_M] - I_d\}^+ \geq I_0$$

In the case of $(I_N + I_M) < I_d$, $\{\ \} < 0$, (14) becomes

$$|I_N - I_M| \geq I_0$$

$$\text{or} \qquad I_N \geq I_0 + I_M \qquad \text{when} \qquad I_N > I_M \tag{15}$$

A characteristic without restraint property is obtained as shown in Fig. 5.

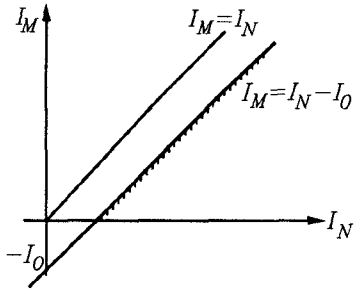

Fig. 5. Characteristic Without Restraint for Smaller Fault Currents $(I_M + I_N) < I_d$

In the case of $\{\ \}+ > 0$, we obtain:

$$I_N - I_M - K(I_N + I_M) + KI_d \geq I_0$$

$$\text{or} \qquad I_N \geq \frac{1+K}{1-K} I_M + \frac{I_0 - KI_d}{1-K} \tag{16}$$

A percentage bias restraint characteristic for an external fault, line rf, according to (16) is shown in Fig. 6.

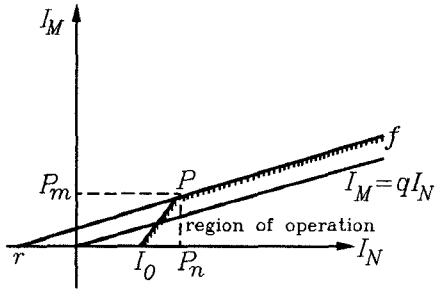

Fig. 6. Restraint Characteristic for External Faults and Internal Fault with Outgoing Current

The criterion (16) can also represent internal fault with outgoing current. Let I_M represent the outgoing current, so that when $\{\ \}^+ = 0$, i.e., without restraint, the characteristic becomes $I_N - I_M \geq I_0$ which is represented by line I_0P in Fig. 6. When $\{\ \}^+ > 0$, the characteristic becomes equal to (16) which is represented by the line Pf in Fig. 6.

Let $q < 1$ be the ratio of the outgoing current to the total incoming current. Then:

$$\frac{1-K}{1+K} = q, \qquad \text{or} \qquad K = \frac{1-q}{1+q} \tag{17}$$

Thus, the restraint characteristic should be:

$$I_N \geq \frac{1}{q} I_M + \frac{I_0 - KI_d}{1-K} \tag{18}$$

The coordinates P_m and P_n of the point P of the restraint characteristics may be obtained by substituting $I_N + I_M = I_d$ into (16). It gives:

$$\left.\begin{aligned} P_m &= \tfrac{I_d - I_0}{2} \\ P_n &= \tfrac{I_d + I_0}{2} \end{aligned}\right\} \tag{19}$$

C. Additional Detection of External Faults

The fault is external if (13) is not satisfied and relay should not operate. For more reliability, an additional detection of external fault and blocking method were adopted. As mentioned above, in the case of an external fault, for example on circuit P, the magnitude of current Δi_{Pk} will be greater than that of all the other currents, and equal and opposite in phase to the sum of them, i.e.:

$$|\Delta i_{P,k}| = max\{|\Delta i_{1,k}|, |\Delta i_{2,k}|, \ldots, |\Delta i_{M,k}|\}$$

and

$$\Delta i_{P,k} = -\sum_{m=1}^{M} (\Delta i_{m,k}) \pm \epsilon \quad m \neq P \tag{20}$$

where ϵ is the maximum error in the CT ratio and data processing before saturation. The relay may be blocked from operation after t_s if (13) was not satisfied and (20) is satisfied after $\Delta i_{p,k}$ was found. This additional detection and blocking measure will increase the reliability of the protection during external faults.

2. Protection Algorithm

In order to minimize the relay operating time, the half cycle integration algorithm is used.

$$S \approx \left[\frac{1}{2}|i_0| + \sum_{k=1}^{\frac{N}{2}-1} |i_k| + \frac{1}{2}|i_{\frac{N}{2}}|\right] T_S \tag{21}$$

thus:

$$I_m = \frac{S \cdot \omega}{2} \tag{22}$$

The total differential current phasor is equal to:

$$I_d = I_1 + I_2 + \ldots + I_n = I_{dm} \sin(\omega t + \alpha) \tag{23}$$

By using (21) and (22):

$$|I_1 + I_2 + \ldots I_n| = \frac{\omega}{2}\left[\frac{1}{2}|i_0| + \sum_{k=1}^{\frac{N}{2}-1} |i_k| + \frac{1}{2}\left|i_{\frac{N}{2}}\right|\right] T_S \tag{24}$$

This algorithm has some filtering effects, but it is not enough, so a band pass digital filter is implemented, which has a pass band of 40–60 Hz. The transfer function of the filter is :

$$H(Z) = \frac{A_4 Z^4 + A_3 Z^3 + A_2 Z^2 + A_1 Z + A_0}{B_4 Z^4 + B_3 Z^3 + B_2 Z^2 + B_1 Z + B_0} \tag{25}$$

where

$$A_4 = 0.003958, A_3 = 0, A_2 = -0.007917, A_1 = 0$$

$$A_0 = 0, B_4 = 1.092933, B_3 = -3.981324, B_2 = 5.624439,$$

$$B_1 = -3.64214, B_0 = 0.914983$$

In the digital form:

$$y(n) = [A_4x(n) + A_2x(n-2) + A_0x(n-4) - B_3y(n-1) - B_2y(n-2) - B_1y(n-3) - B_0y(n-4)]/B_4 \quad (26)$$

Fig. 7 shows the frequency response characteristic of the filter.

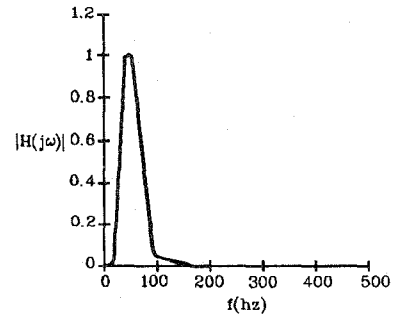

Fig. 7. Frequency Response of the Band Pass Filter

RELIABILITY COMPARISON

There are two main differences between the distributed bus protection principle and the traditional centralized principle, namely:

- A number of separately installed protection units supersede one centralized protection device.
- A data communication network is used instead of direct connection of the CT's secondary cables.

The reliability may be compared around these two points. The probability of maloperation increases with the increase of the number of devices, but the probability of the entire bus protection non-operation decreases with the number of devices. The severe consequence of the entire black-out of the high voltage bus system, time required for its restoration, loss of energy, etc., is much worse than maloperation of one protection unit causing service interruption of only one circuit. Similarly, other consequences of non-operation of the centralized bus protection causing further damage of the equipment may also be much worse when compared with the consequence of non-operation of only one protection unit on one circuit.

As to the wiring complexity, the IEEE-488 bus is only a communication cable with 25 wires. The connection of the protection units by this communication cable is very simple as compared with wiring of a number of CT secondary cables.

A modern data communication network has very high reliability, the error rate is as low as 10^{-9}. For a transmission speed of 10 Mbps, this equals one bit error in 100 seconds of continuous transmission. Time for protection to operate is about 30 ms in average. In this short period, the probability of the appearance of 1 bit error is $\frac{30}{100000} = 3 \times 10^{-4}$. With the help of the error detection and error correction algorithms, the transmission error will not cause incorrect operation of the relay.

To sum up the above preliminary comparison, the proposed distributed bus protection possesses indeed a high reliability.

DESIGN AND TEST RESULTS

Such protection unit is designed to be an integrated device consisting of 8 modules: AC input module, status signal input module, data acquisition and A/D conversion module with single chip microprocessor Intel 8797BH (CPU1), data communication module with processor 8976BH (CPU2), protection module with fast data processor TMS320C30 (CPU3), tripping and signaling relay module, man machine interface module with processor Intel 8098 (CPU4) and DC power supply module.

For verification of the principle, especially of the data communication network, four such protection units were made and mounted on four circuits connected to the protected bus as shown in Fig. 8. The test is based on the following characteristic, which has a better restraint property than formula (14):

$$|I_1 + I_2 + \cdots + I_M| - K_1\{|I_1| + |I_2| + \cdots + |I_M| - K_2|I_1 + I_2 + \cdots + I_M| - I_d\}^+ \geq I_o \quad (27)$$

Faults on a circuit (circuit No. 4) outside the protected bus (F_1), and on the protected bus (F_2) were made. The four protection units all operated correctly.

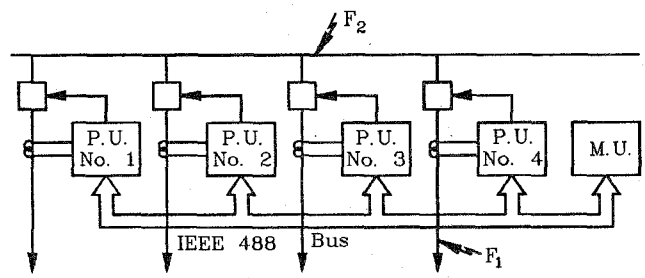

Fig. 8. Experimental Circuit Connection
P.U. – Protection Unit M.U. – Monitoring Unit

The current data from one phase (phase A) of protection unit No. 1, and from the other three circuits, are received by the protection unit No. 1 from the communication network and stored in the two port RAM of protection unit No. 1. This data is shown in Table I (for short circuit outside the bus) and Table II (for short circuit on the bus). Table I shows that for short circuit outside the bus, the differential current calculated by the protection unit No. 1 (the sum of the four current instantaneous values), produced by the unbalance of the CTs and transmitting

Table I. Samples of the Phase A Currents Received by Protection Unit No. 1 from Communication Network; Differential Current and Restraining Current Calculated in Case of External Fault (F_1)

No. of Samp	P.U. No. 1 (A)	From P.U. No. 2 (A)	From P.U. No. 3 (A)	From P.U. No. 4. (A)	Diff. Cur. (A)	Rest. Cur. (*) (A)
1	4.392	7.466	14.347	-25.766	0.439	51.094
2	5.270	7.759	14.493	-27.230	0.292	54.168
3	5.417	8.052	14.201	-26.645	1.025	52.265
4	4.978	6.881	12.298	-23.278	0.879	45.677
5	3.953	5.417	10.248	-19.325	0.293	38.357

(*) Restraint Factors $K_1 = 1$, $K_2 = 2$

errors, is very small, so that the protection does not operate. Table II shows that for the short circuit on the bus, the calculated differential current is large and the protection operates. The experiment on such model bus shows that the proposed distributed principle of bus protection is possible and may work satisfactorily.

Table II. Samples of the Phase A Currents Received by Protection Unit No. 1 from Communication Network; Differential Current and Restraining Current Calculated in Case of a Fault on the Bus (F_2)

No. of Samp	P.U. No. 1 (A)	From P.U. No. 2 (A)	From P.U. No. 3 (A)	From P.U. No. 4. (A)	Diff. Cur. (A)	Rest. Cur. (A)
1	2.342	4.099	4.392	5.563	16.396	0
2	3.074	4.831	5.710	7.027	20.642	0
3	3.514	5.124	5.563	8.345	22.546	0
4	3.514	4.978	6.588	8.491	23.571	0
5	2.928	4.099	6.002	7.759	20.788	0

CONCLUSIONS

1. The distributed bus protection principle proposed in this paper possesses improved reliability over the traditional principle. It enables full elimination of a serious blackout of the whole bus due to misoperation of the protection.
2. The IEEE–488 standard bus adopted can fully satisfy the demands of the proposed distributed bus protection system for real–time data communication. It also enables the protection system to use the information of the whole substation and power system to enhance its adaptability.
3. As the protection CPU TMS320C30 has particular ability and high speed in data processing, it executes not only the full protection programs, but also does many tasks in error detection and correction, data estimation, bad data elimination, etc., to ensure the correctness of the protection system operation.
4. Experimental results show that this bus protection principle is feasible and possesses distinguishing advantages over traditional centralized principle.
5. Unfortunately, since the CT model with the ratio 15:5 used in the laboratory does not simulate the saturation performance of the real CT, the saturation test was not conducted. The percentage bias characteristic adopted is widely used in practice. It can prevent maloperation of the relay for external faults. In fact, the relay will be blocked before CT saturation when the external fault is detected by (20).

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