

## NEW DIGITAL SIMULATOR DESIGNS FOR PROTECTIVE RELAY TESTING

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**Abstract**— This paper discusses results of several research and development activities related to digital simulators for relay testing. Extensive hardware and software have been developed and used for implementation of various simulator configurations. Each of the configurations are described and their characteristics are presented.

**Keywords:** Digital Simulators, Protective Relaying, Relay Testing, EMTP

### INTRODUCTION

Use of power system simulators in relay testing has been a practice for a long time [1]. However, this practice has primarily been established by relay manufacturers and large utilities based on their capability to justify a substantial cost associated with developing and implementing a transient simulator. A real technical challenge was to develop a simulator for relay testing which would be affordable for a wide spread use and yet flexible enough to carry out the required test procedures.

Several attempts were made in the past to improve flexibility of the existing analog simulators by providing computer controlled support for configuring test systems, executing tests and analyzing the results [2]. Further improvements were made by introducing hybrid simulators which have utilized analog and digital electronic components [3]. This approach has reduced somewhat the cost of implementation and yet additional flexibility of setting

up simulations and the possibility of achieving required accuracies were introduced.

However, a major breakthrough in the simulator development was achieved by using extremely flexible digital simulation technology, high precision D/A design techniques, and advanced power amplifier features.

As a result, several digital simulator designs have been introduced in the last ten years. They have been implemented in a number of different ways ranging from PC-based [4] to workstation-based [5] designs. Some of the latest designs are based on advanced parallel [6] and distributed processing [7] architectures.

This paper presents the results of some recent development projects sponsored by the Electric Power Research Institute (EPRI) and several major U. S. utilities. The intent of the sponsors was to develop digital simulator configurations with low and moderate cost options that would meet a wide range of technical requirements. Such an approach has been achieved through two separate developments. One sponsored by the Electric Power Research Institute (EPRI) and another by DOE-Western Area Power Administration (WAPA). Both developments were carried out by the research staff of the Electrical Engineering Department of Texas A&M University.

The paper first discusses relay testing requirements. Then, simulator design requirements are defined. After that the goals of each of the projects are outlined. Development of common hardware is discussed next. Application software options are also presented. Finally, different simulator configuration possibilities are specified at the end.

## **RELAY TESTING REQUIREMENTS**

Relay testing requirements can be classified in two broad categories:

- Design Verification Testing
- Application Evaluation Testing

Design verification testing is aimed at evaluating basic relay performance features such as operating characteristics and operating times. A reference for this testing is a set of design parameters defined by the manufacturer. The present practice followed by almost all the manufacturers is to provide phasor-based operating characteristics for steady-state and some dynamic conditions. Therefore, most of the design verification testing is aimed at verifying these characteristics. In order to be able to generate the required test waveforms, voltage and current signals should be adjustable both in phase and amplitude. A typical requirement is that the test waveforms are representing pre-fault, fault and post-fault phasors. It is important that the transitions from one phasor state to another are performed in a "smooth" way without introducing artificial transients. Synchronous change in the phasor parameters for all of the test signals is also a requirement. This testing is often denoted as phasor testing.

Application evaluation testing is a far more complex stage than design verification testing. The application conditions assume that a relay is subjected to actual fault transients. The actual fault transients can be obtained using either fault records captured in the field by a Digital Fault Recorder (DFR), or simulated fault waveforms generated by an Electromagnetic Transient Program (EMTP). In both cases, the transient waveforms will depend on the network type, fault characteristics, loading conditions and type of relaying transformers used. It is, therefore, essential that application evaluation testing is performed using as accurate as possible fault waveform representation. This testing is very often denoted as transient testing.

Transient testing may be applied in at least two different ways. One is to perform a sensitivity study where certain waveform characteristics are varied and relay responses are observed. A typical example is evaluation of relay responses for different fault conditions where one of the following signal and/or fault conditions are being varied: DC offset, fault resistance, fault location, fault incidence angle, fault type.

Yet another way to perform transient testing is to subject a relay to the test waveforms representing a given fault condition. In that case, a trip/no trip condition is observed as

well as the tripping times.

### SIMULATOR DESIGN REQUIREMENTS

As a result of the relay testing requirements, several important digital simulator design requirements can be defined. A summary of these requirements is given in Table I.

**Table I. Simulator Design Requirements**

<b>Design Requirements</b>	<b>Relay Test Requirements</b>
One and Multi-terminal Configuration	Both Phasor and Transient Testing
Synthesized Test Waveform Generation	Both Phasor and Transient Testing
Phasor Variation	Phasor Testing
Transients Variation	Transient Testing
Signal Processing and Analysis	Sensitivity Study
Real-Time Interaction	Relay Evaluation for an Autoreclosing Sequence
Accurate Instrument Transformer Representation	Relay Evaluation for a Given Fault
Flexibility in Setting Up Test Cases	Repetition of a Large Number of Tests
Graphical User Interface	Building of Test Cases; Representation of Test Results
Multi-User, Multi-Tasking Computer Environment	Multiple Operators with Several Concurrent Test Preparation Jobs

The number of relay terminals to be tested simultaneously ranges typically from one to three. Single terminal testing is related to evaluation of a single relay. Two terminal testing is used to evaluate relaying schemes consisting of two relays. An example are relays located at two ends of a transmission line. Three terminal testing is specifically needed when coordination of three relays is evaluated. Examples include testing of relay operations on tapped lines or parallel lines.

One of the main relay testing requirements is a flexibility in producing test waveforms. This translates into a requirement to have at least three different ways of generating these waveforms: synthesizing waveforms from mathematical expressions, producing phasors by a simulation, and producing transients from a simulation or a recorded fault waveform.

Signal processing and analysis is an extremely important feature when an operator wants to alter waveform characteristics and to observe waveform properties. Obviously, this step is only possible in an open-loop mode of relay testing where a relay is subjected to a given set of test waveforms and a response is observed. In this case, an operator can intervene by processing and analyzing test waveforms before they are outputted to the relay.

A different situation occurs when it is important to evaluate relay operation after network conditions have changed due to an initial relay operation. A typical example is evaluation of relay operation under autoreclosing conditions. In this case, a real-time interaction between the relay and the simulator needs to be provided. The test sequence is executed in small fractions of a second and any operator intervention in altering waveforms can not be accommodated.

The influence of instrument transformers on relay operation is quite important since these transformers act as nonlinear filters. This influence has the greatest impact when a relay's performance under actual fault conditions is being evaluated. In design verification testing, instrument transformers may only be represented as ideal elements with different turn ratios.

Flexibility in setting up test cases, the graphical user interface, and the multi-user, multi-tasking environment relate to the efficiency of carrying out relay testing when a large number of tests needs to be performed. Experience shows that well over a thousand tests may be needed to fully evaluate a complex line protection relay. The support for an operator to carry out such a large number of tests becomes extremely important. The computer environments used for the simulator implementation play a major role in providing the required capabilities.

## SIMULATOR PROJECTS

A need to study simulator issues was recognized by EPRI and several of its utility members in 1989. A research project was initiated (EPRI RP 3192-01) to investigate major issues in digital simulation such as modeling of network faults, instrument transformer modeling, high precision D/A subsystem requirements, and DC-coupled power amplifier specifications. As a result of this effort, several software and hardware enhancements for open-loop digital simulators were developed and guidelines for digital simulator use in relay testing were outlined [8]. The first phase of this project resulted in a PC-based version of a new open-loop simulator design demonstrated in July of 1992. A beta version was delivered to FPL in 1993.

As a result of a successful completion of Phase I, EPRI and some of its utility members sponsored further simulator developments as a part of Phase II of the project. The main goal of this phase is to implement a workstation-based version of the open-loop simulator providing major enhancements in the user interface capabilities. These activities are underway and are scheduled for completion in 1995.

Finally, another simulator project was initiated by DOE-Western Area Power Administration (WAPA) in 1989 and a contract for simulator development was awarded by the end of 1990. This project was aimed at developing an advanced real-time version of a digital simulator design. The first phase of this project was devoted to a feasibility study of such an advanced design which is technically quite involved. An approach to the simulator implementation had been defined in the Spring of 1992 and a version of the real-time simulator has been developed and implemented by the Summer of 1993. The simulator is undergoing final testing and is ready for delivery to Western Area Power Administration in the first quarter of 1994.

## COMMON HARDWARE APPROACH

In order to be able to discuss the common hardware developments, a generic hardware architecture of a simulator is shown in Fig. 1.

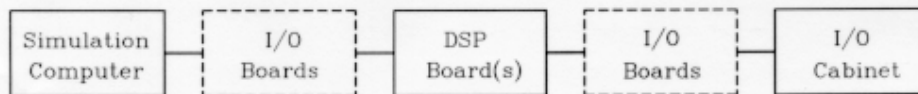


Fig. 1. Generic Hardware Architecture

The simulation computer can either be a PC or an IBM RISC 6000 workstation. The choice of the computer is related to the choice of the application software. The PC-based simulator is always an open-loop design while the real-time design always requires a high performance IBM RISC 6000 machine. However, an open-loop design can also be implemented using an IBM RISC 6000 workstation.

The I/O boards between the simulation computer and the DSP computer were developed for the IBM RISC based workstation since there were no DSP boards available on the market that will plug into the Microchannel bus. In the case of a PC-based simulator, such DSP boards are available and there is no need to use separate interface boards.

The DSP boards used in the design are commercial products. Their required computing power and application role may be different in the case of the PC-based versus RISC-based simulator.

The PC-based, open-loop, configuration uses a DSP board containing a TI C30 chip. The role of this board is to provide parallel-to-serial conversion which is needed when data is sent from the simulation computer to the relay under test. The RISC-based configuration uses a more powerful DSP board with two TI C40 DSP chips per board. The open-loop simulator requires one DSP board while the real-time design requires two DSP boards. The PC-based simulator can also be configured using the high performance DSP board if the choice is to utilize the additional computing power for some application software implementation on the DSP board. In all of the mentioned cases, different application software has been developed for various application needs. This will be discussed further in the software section of the paper.



The I/O board between the DSP board and the I/O cabinet is only needed in the case that the advanced version of the DSP board with two DSP chips is used. In the case of a configuration with the powerful DSP board(s), the I/O board converts the parallel data generated by the DSP to the serial data accepted by the I/O cabinet. In the case of a PC-based simulator using the C30 based DSP board, the serial output of the DSP board is directly used to interface to the cabinets and there is no need for a separate I/O interface board.

**Table II. Typical Characteristics of the I/O Cabinet**

ITEM	SPECIFICATION
# of Reproduced Bits	16
Sample Rate	$F_s=3.2$ to 25 kHz
Output Impedance	Voltage Channels: $< 1\Omega$ Current Channels: $> 500\Omega$ ; DC to 1 kHz
Analog Bandwidth	DC $\rightarrow$ 0.45 fs
Output Signal Range	Voltage Channels: $> \pm 320V_{peak}$ ; $\pm 0.2A_{peak}$ Current Channels: $> \pm 160A_{peak}$ ; $\pm 100V_{peak}$
# of Analog Channels	12 Voltage + 12 Current*
# of Digital Channels	48 Input + 48 Output**
Channel Skew	$< 1\mu s$

\* 3 sets of 4 voltage and 4 current channels each.

\*\* 3 sets of 16 input and 16 output channels each.

Finally, the last item is the I/O cabinet. This cabinet contains a high precision D/A conversion subsystem and high power DC-coupled voltage and current amplifiers. The cabinet design has been developed under the EPRI project and has been used for both open-loop and real-time simulator designs. It represents a very accurate waveform replay system. Some typical performance data for this design are given in Table II.

It is important to recognize that some of the properties of the hardware design are common for all of the simulator configurations. In all the configurations it is possible to use up to three I/O cabinets allowing for testing of up to three relay terminals. Also, in all configurations, the links between the simulator computer and the I/O cabinet are bi-directional. Outputs of the simulation computer are analog waveforms and contact data.



The inputs to the simulator computer are contacts that are generated by the relay under test.

An important feature of the common hardware approach is that all the simulator designs are upward compatible. This means that a PC-based simulator can be upgraded to an open-loop RISC-based simulator by changing the computer and the DSP boards. Once this is done, only the RISC-based software upgrade is needed to have a high performance open-loop simulator. The next upgrade is from an open-loop RISC-based simulator to a real-time RISC-based simulator. This requires one more (high performance) IBM RISC 6000 computer, one more DSP board and a software upgrade. The software upgrade will require different application and system software, but this code will run on the new simulator configuration consisting of the open-loop simulator hardware and the newly added hardware. Obviously, one possibility is that a user of the real-time simulator can run both the open-loop, and the real-time software on the real-time simulator configuration.

#### **APPLICATION SOFTWARE OPTIONS**

The main module of the application software in all of the simulator configurations is an electromagnetic transient program. The open-loop simulator options can use standard electromagnetic transient programs such as EMTP-DCG distributed by EPRI [9]. This program comes in both a PC and an IBM RISC 6000 version. The program has an input interface called EMTP-IN and an output graphics display interface called EMTP-OUT. This is quite a powerful simulation program that can be used to simulate a number of different cases/options needed in the relaying studies.

The real-time simulator design can not use the standard EMTP software due to the computational constraints imposed by the real-time operation. A separate Real-Time System (RTS) software had to be developed, based on the same underlying theory as used in the EMTP, to achieve the computational efficiency needed for the real-time operation. This program is tailored for relaying studies, and as such, only contains the models of the network components that are most interesting for the relaying studies. A summary of the component models available in the RTS software [7] is as follows:

- Uncoupled branches:  $R, L, C$  and  $R - L$
- Coupled  $R - L$  branches
- $\Pi$ -circuits for short lines representation
- Constant parameter overhead transmission lines
- Transmission lines with frequency dependent parameters
- Voltage sources
- Faults
- Relays
- Switches and circuit breakers
- Series capacitors with MOV protection
- Surge arresters
- Instrument Transformers: CTs and CCVTs

Finally, it was recognized that a custom designed Graphical User Interface (GUI) for an electromagnetic transient program would be a desirable approach for setting the models and running the simulations. A dedicated GUI was developed for the RTS software and a similar development is planned for the EPRI EMTP software.

Other important software modules are file conversion software and signal processing software [10]. Both of these packages were developed for the open-loop simulator design. After describing the role of each of these packages, it will become apparent that these packages are only applicable to open-loop relay testing.

The file conversion software is written in C-language and can be used on either the PC- or the RISC-based simulator configurations. This software enables conversion of the

EMTP output files, as well as the Digital Fault Recorder (DFR) files to be used by the signal processing package. Obviously, this enables the use of a number of different electromagnetic transient programs as well as a number of DFRs. The conversion software accepts ASCII output files from EMTP-DCG, EMTP-BPA, ATP and MICROTRAN versions of the electromagnetic transient program. Binary output files from the following DFRs can also be converted: Hathaway, Rochester, Mehta Tech, Utility Systems. The conversion software can also accept the files in the standard COMTRADE format [11]. In all the cases, different data formats of the test signals are converted to the format of the commercial package used for the signal processing functions.

The signal processing is implemented using a commercial package called MATLAB [12]. A number of functions aimed at signal processing and signal analysis were developed specifically for the relay testing purpose. Various modules of this software are presented in Fig. 2. A detailed description of each of the modules is given in reference [10].

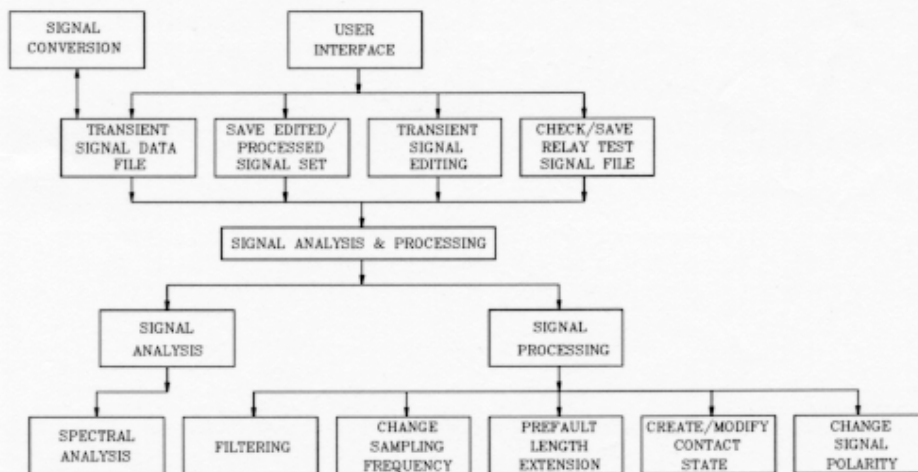


Fig. 2. Signal Processing Software Modules

Finally, application software modules for the simulation of instrument transformer

and circuit breaker models have also been developed. As is well known, simulation of these components is extremely important in the relaying studies and a special care was given to the accuracy and flexibility in implementing the models for those components. Two different software implementations were developed, one for the open-loop simulation and the other one for the real-time simulation.

The open-loop simulator implementation of instrument transformers and circuit breakers was done as a part of the EPRI EMTP program. New detailed models of several capacitor coupling voltage transformers (CCVTs) were developed after an extensive study of their frequency responses was conducted under the EPRI sponsorship [13–15]. An evaluation of the existing current transformer (CT) models, that can be constructed using the EMTP program, was also performed under the EPRI sponsorship by comparing high-power laboratory tests with EMTP simulations [16].

The real-time simulator implementation of the instrument transformers is based on the published results from the EPRI study. However, these models are implemented on the DSP boards using highly computationally efficient assembly language code. In addition, a special model of circuit breaker logic developed specifically for the real-time simulator. It is was also implemented on the DSP boards using assembly language.

### SIMULATOR CONFIGURATIONS

A block diagram for the generic simulator configuration is given in Fig. 1. Based on this figure, a configuration guide for hardware and application software is given in Table III. A block diagram of some typical configurations is given in Fig. 3.

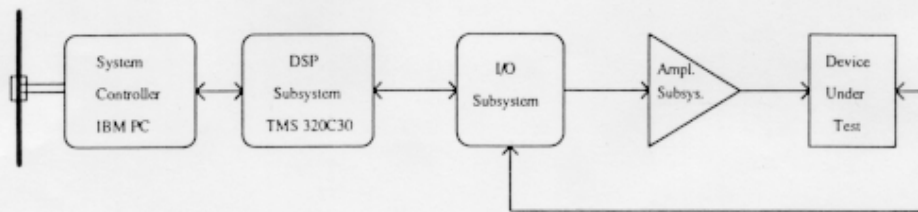
As it can be observed, the simulator configuration options are compatible and upgradable so that a user can choose to start with a PC-based configuration, which is a low-cost high performance open-loop test system. Over a period of time, this configuration can be upgraded to a higher cost, higher performance RISC-based open-loop test system. Eventually, a real-time test system can be configured purchasing software and hardware upgrades. This design flexibility allows for a phased financial investment and also a step-

by-step upgrade of testing complexity. This feature is considered quite important since it allows users to make a gradual transition from their present relay test practices into more advanced transient testing using digital simulators.

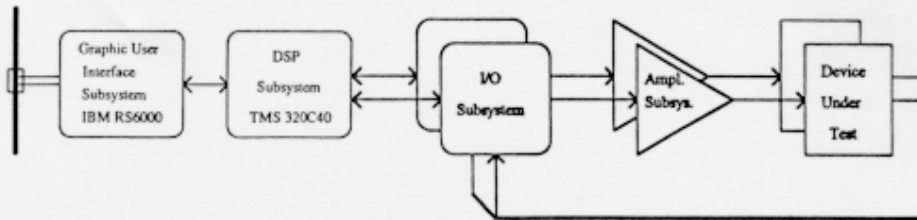
Finally, it shall be observed that different system support software needs to be installed on each of the configurations to be able to utilize the same base hardware while making only upgrades in the additional hardware and the appropriate application software.

**Table III. Configuration Guide for Digital Simulators**

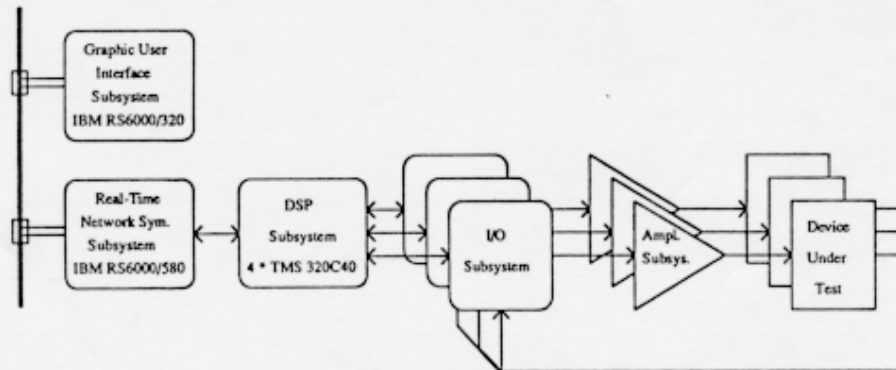
Hardware/Software	Open-Loop	Open-Loop	Real-Time
	PC-Based Config.	RISC-Based Config.	RISC-Based Config.
PC	X	-	-
IBM RISC 6000 (Low Performance)	-	X	X
IBM RISC 6000 (High Performance)	-	-	X
TI C30 DSP	Option 1	-	-
TI C40 DSP (Two Chips per Board)	Option 2	One Board	Two Boards
RISC-to-DSP Interface	-	X	X
DSP-to-Cabinet Interface	Option 2	X	X
I/O Cabinet	Up to three	Up to three	Up to three
EMTP	X	X	-
RTS	-	-	X
GUI	Planned	Planned	X
Signal Processing	X	X	-
Instrument Transformers	X	X	on the DSP Board
Circuit Breakers	-	-	on the DSP Board
Open-Loop System Support	X	X	-
Real-Time System Support	-	-	X



(a) PC-Based Single Terminal Open-Loop Configuration



(b) RISC 6000-Based Two Terminal Open-Loop Configuration



(c) RISC 6000-Based Three Terminal Real-Time Configuration

Fig. 3. Typical Digital Simulator Configurations

## CONCLUSIONS

Based on the information presented in the paper, the following can be concluded:

- Low Cost, High Performance Transient Simulators are Feasible
- Relay Test Requirements May Vary
- Digital Simulator Design Presented Enables Portability and Upgradeability
- This Design is Based on Commercial Hardware and System Software with a Custom Designed Application Software

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## REFERENCES

- [1] CIGRE WG Report, "Dynamic Test Procedure for Static Line Protection," CIGRE Paper 34-08, *CIGRE General Session*, September 1980.
- [2] R. E. Ray, H. J. Li, "A Computer Controlled Model Power System," *Western Protective Relaying Conference*, Pullman, October 1986.
- [3] G. Nimmersjo, et. al., "A Digitally-Controlled Real-Time Analog Power System Simulator for Closed Loop Protective Relaying Testing," *IEEE TPWRD*, Vol. 3, No. 1, January 1988.
- [4] M. A. Redfern, et. al., "A Personal Computer Based System for the Laboratory Evaluation of



Performance Power System Protection Relays," *IEEE TWRPD*, Vol. 6, No. 4, 1991.

- [5] M. Kezunović, et. al., "DYNA-TEST Simulator for Relay-Testing - Part I: Design Characteristics," *IEEE TPWRD*, Vol. 6, No. 4, 1991.
- [6] P. G. McLaren, et. al., "A Real-Time Digital Simulator for Testing Relays," *IEEE TPWRD*, Vol. 7, No. 1, 1992.
- [7] M. Kezunović, et. al., "Transients Computation for Relay Testing in Real-Time," *IEEE PES-Summer Meeting*, Paper No. 93SM 383-0-PWRD, Vancouver, B. C., Canada, July 1993.
- [8] M. Kezunović, "Protective Relay Workstation - Application of Digital Simulator for Protective Relay Studies," *Electric Power Research Institute RP 3192-1, Phase I Final Report*, Palo Alto, California, October 1993.
- [9] *Electromagnetic Transient Program (EMTP) Rule Book EPRI EL-6421-I*, Vol. 1, 2, Research Project 2149-4, June 1989.
- [10] M. Kezunović, et. al., "Advanced Signal Processing and File Management Software for Relay Testing Using Digital Simulators," 11<sup>th</sup> *PSCC*, Avignon, France, September 1993.
- [11] IEEE Standard C 37.111-1991, *Common Format for Transient Data Exchange (COMTRADE) for Power Systems*, IEEE Service Center, 1991.
- [12] "386-MATLAB," *Instruction Manual*, The MathWorks, Inc., South Natic, MA 01768, May 1989.
- [13] M. Kezunović, et. al., "Digital Models of Coupling Capacitor Voltage Transformers for Protective Relay Transient Studies," *IEEE TPWRD*, Vol. 7, No. 4, pp. 1927-1935, October 1992.
- [14] Lj. Kojović, M. Kezunović, et. al., "A New Method for the CCVT Performance Analysis Using Field Measurements, Signal Processing and EMTP Modeling," *IEEE PES Winter Meeting*, Paper No. 94 WM 003-4 PWRD, January 1994.
- [15] Lj. Kojović, M. Kezunović, S. L. Nilsson, "Computer Simulation of a Ferroresonance Suppression Circuit for Digital Modeling of Coupling Capacitor Voltage Transformers," *ISMM Conf. on Computer Applications in Design*, Orlando, March 1992.
- [16] M. Kezunović, et. al., "Experimental Evaluation of EMTP Based Current Transformer Models for Protective Relay Transient Study," *IEEE PES Winter Meeting*, Paper No. 041-4 PWRD, January 1993.