A New Multiprocessor Architecture Implementation of a Real-time Simulator for Power System Applications

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1. Introduction

The use of digital simulators for power system protection applications has been known since the early eighties. A number of different designs have been introduced over the last ten years. These simulators have been proven to be very accurate and flexible tools for relay testing [1,2]. However one limitation of the mentioned designs was difficulty in performing relay testing in real-time. Digital simulators of an open-loop type are extremely effective in producing fault transients by replaying either simulated or recorded transients into relays for testing purposes. Nevertheless, if the relay testing requires multiple dynamic changes of the power system configuration based on the relay's response, the open-loop simulators can not support real-time interaction between the power system model and the actual protection relay under test.

Several recent papers have investigated fast methods for computation of power system transients [3-5]. It has been argued that parallel computer architecture is needed to meet the real-time computation requirements [5,6]. Those feasibility study results are encouraging for future implementations. A complete design of a simulator suitable for relay testing has recently been demonstrated. The system uses a custom computer design. The reported development is very important since it proved the validity of a parallel architecture approach [6].

This paper describes development of a new digital simulator with very stringent implementation requirements [7]. The use of commercially available computer architecture was favored against the use of a customized solution. Such an approach enables the simulator to take full advantage of existing system software and hardware support , as well as upgrades readily available for commercial computer products.

The first part of the paper is devoted to a discussion of the simulator design requirements. The next section gives an overview of the system architecture. The simulator performance evaluation methodology and results are provided at the end.

2. Design Requirements

The basic design requirements may be grouped as follows:

- Graphical User Interface (GUI)
- Real-Time Simulation (RTS)
- Waveform Reconstruction System (WRS)

The GUI requirements ask for a highly interactive work environment. It is required that most of the data entry tasks are carried out by direct manipulation of the icons displayed on the screen, using a mouse.

The GUI is needed to enter data that relates to power system simulation. This data describes power system network components, their connections and their parameters. Therefore, the interface needs a drawing capability to create a network and a menu capability to enter the network component parameters. Extensive editing is also needed for manipulation of various network components.

The RTS requirements are related to simulation of transients in a power system network. The transients are caused by faults in the actual networks, which is commonly recognized as electric power outage in a given section of the system.

Transients are detected by protective relays, the devices that are to be tested with the digital simulator. Signal sensing is done through relaying transformers which include current transformers (CTs), potential transformers (PTs) and capacitor coupling voltage transformers (CCVTs). Once the protection relays have detected a fault, they operate circuit breakers that disconnect the faulted section of the power system. Also, the relays interact with each other through a communication link. In this way, relays at two or three different transmission line ends act as a system. To test

such a relaying system, two or three terminal simulator configurations are needed.

This brief outline of the RTS requirements indicates that the simulation of power network faults requires different models as follows: network components, instrument transformers, and circuit breakers.

Design requirements of the RTS for network components have been defined based on a set of representative network sections of the Western Area Power Administration (WAPA) system. A typical network configuration is given in Figure 1.

The equivalent circuits for the network have between 30 and 60 nodes. The levels of description of individual network components range in complexity, from a simple RL element branches, to a complex distributed parameter frequency dependent overhead transmission lines. In the latter case, both the characteristic impedance and propagation function of a single line can be described by transfer functions having up to 25 poles and covering the frequency range up to several MHz.

The simulator real time performance was to be proved on several benchmark cases defined in advance. Computations of an average case from the set of benchmarks is equivalent in its linear part to integration of a set of over 200 linear differential equations. In addition to that, the RTS in the given case must provide for computing of over 10 nonlinear components, and must accommodate changes in the network topology resulting from relay controlled circuit breaker operations.

The target time step computation times were set from 50 to 110μsec depending on the benchmark case.

The network simulation requirements discussed fall into a category of requirements defined for some commercial programs, such as the Electromagnetic Transients Program (EMTP). These programs are well known in the power industry and have been used for a number of different applications [8-10]. However, these programs are not designed for real-time operation. Network simulation requirements discussed in this paper are, therefore, quite unique since the real-time performance is the key requirement.

Design requirements for the real-time instrument transformer implementation follow from the models of the devices, as discussed by the authors in earlier publications [11,12].

The Current Transformer (CT) model is a simple network. One of the branches contains a nonlinear element described by a piecewise linear characteristic. A single step solution of the CT model involves solving the linear part and searching the nonlinear characteristic to find the correct segment.

The Capacitor Coupling Voltage Transformer (CCVT) model is a linear circuit with 5 nodes and 12 branches. A single step solution of the CCVT model can be carried out either by solving the circuit for all voltages and currents or by using a difference equation representing an equivalent IIR filter. Even though the latter approach is more natural to the implementation on a digital signal processor, the former is preferable due to the advantage of all voltages and currents in the circuit being available as program variables and the possibility of future upgrades by incorporating nonlinear elements.

The WRS requirements, relate to reconstruction of voltage and current analog signals based on the digital samples of these signals produced by the RTS system.

Once the network transients are generated, these transients need to be submitted to the device being tested. Likewise, any reaction from these devices has to be fed back into the simulator. This interaction places a unique set of requirements on the I/O interface subsystem as shown in Table I.

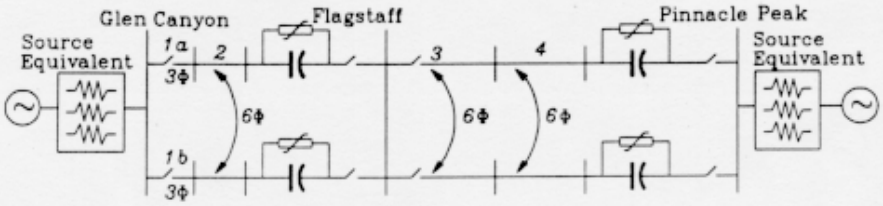

Figure 1. Typical Network Configuration for WAPA System

Table I. Waveform Reconstruction System Performance Requirements

	Parameters	System Performance
1.	Number of Analog Channels	3 Current + 3 Voltage (4+4)
2.	Output Signal Range	>±325V peak; >±200mA peak - Voltage >±160Apeak; >±100Vpeak - Current
3.	Analog Bandwidth	DC to 0.45 fs; ±0.5dB
4.	Number of Reproduced Bits	16 bits
5.	Sample Rate	Variable: fs = 3.2 to 35 kHz
6.	Output Impedance	< 1Ω -Voltage Outputs (DC to 17 kHz) >500 Ω - Current Outputs (DC to1 kHz)
7.	Number of Digital Channels	16 Input + 16 Output

3. System Architecture

The new simulator system architecture is shown in Figure 2. The system is made of the following major components:

- IBM RISC System /6000, Model 320, supporting the Graphical User Interface (GUI)
- IBM RISC System /6000, Model 580, supporting the real-time network computation
- Digital Signal Processing (DSP) subsystem supporting the real-time modeling of instrument transformers
- Waveform Reconstruction System (WRS) supporting real-time Input / Output (I/O) interaction between the simulator and the relays under test.

The GUI subsystem enables the operator to enter the network configuration and parameters needed for simulation. Data entry is performed off-line with respect to the real-time simulation. Therefore, there are no interactions between the GUI and RTS once the real-time simulation is initiated. After the simulation is completed, the test results are collected and displayed to the operator by the GUI.

The real-time network simulation (RTS) subsystem, at a request from GUI, reads a file containing a full description of the simulation case. A typical simulation case is centered around a fault event (a short circuit condition) which is introduced in the system at a given time. The simulation proceeds in two stages; pre - fault and post - fault. In the pre - fault stage, the RTS computes steady state values of the system. Aside from being a natural initial state, the pre - fault stage serves to initialize the models realized on the DSPs as well as the relays being tested. At the user's request, the RTS inserts the fault condition and proceeds to post - fault stage.

The post - fault stage is critical for the simulation performance as it involves the bulk of the computational effort. The complexity of the computations is accentuated by the fact that the system under study may contain nonlinear components and overhead transmission lines with frequency dependent parameters.

The DSP subsystem contains 2 boards hosting a total of 4 TMS320C40 processors. Three of the processors are allocated to the modeling of instrument (current and potential) transformers and the I/O subsystem communication link control. The fourth device performs housekeeping functions, modeling of the circuit breakers,

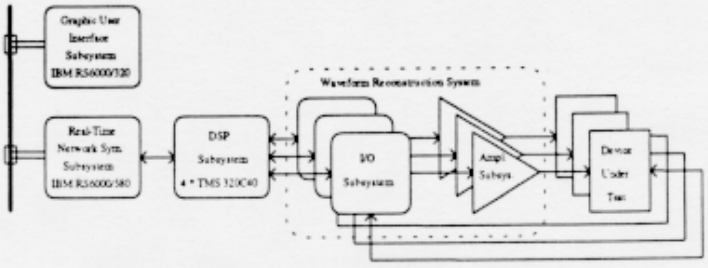

Figure 2. Real-Time Simulator System Architecture

and the communication with the IBM machine executing the primary network model.

Special attention was given to detailed instrument transformer modeling. Recent studies conducted by the authors [11,12] indicate that the measurement devices normally used to monitor the high voltage primary network can have significant influence on the output waveforms. This can be explained by the fact that these devices are last in the signal chain and are directly connected to the relays.

The waveform reconstruction system contains all of the components necessary for interfacing between the simulation computers and the external (analog) world. Special attention was given to the system modularity, and high output waveform signal precision. This was achieved by placing 6 D/A converters and their associated reconstruction filters (I/O subsystem) together with a set of 3 current and 3 voltage amplifiers. The devices are placed inside a standard 19 inch rack cabinet. One cabinet contains all of the hardware necessary for testing of a single protection device. Up to 3 cabinets can be connected together forming a 3 terminal real-time simulator shown in Figure 2. The same cabinets are used in an open-loop (replaying) based simulator system.

The cabinets use bi-directional digital data links providing reliable communication between the relays and the computer system. In addition to the modularity, the integration of the waveform reconstruction hardware into a single 19 inch cabinet, enabled tight output signal precision control, minimized crosstalk, and minimized interference problems associated with high output current levels.

4. Hardware / Software Techniques

In order to achieve real-time operation and satisfy the demanding sampling frequency requirements, the simulator uses several hardware and software optimization techniques. The required speed was achieved by:

- Development of new network component models and solution techniques amenable to real time execution.
- Shifting, as much as possible, the computational burden to the preparatory phase of a simulation run.
- Development of an optimized C code of the RTS that is tuned to the architecture of IBM RISC 6000/580 machine.
- Use of inherent network simulation parallelism by decoupling the instrument transformer models and allocating them to dedicated DSP processors.
- Development of an optimized assembly language implementation of the instrument transformer models for high speed DSP execution.
- Minimization of data communication and synchronization overhead.

Special attention was given to the real-time operating system issue. The IBM RS6000 series machines normally run under AIX, the IBM enhanced version of the UNIX operating system streamlined by using explicit locking of all shared data structures used by the core. This results in a highly efficient real-time application support. The system provides all of the necessary memory locking primitives, and reasonably fast interrupts [13]. However, the required context switch time limits the maximum application sample rate to approximately 1 kHz, falling short of satisfying the stated 20 kHz sample rate requirement.

The problem was solved by temporarily shutting down the operating system core, and passing the full control to the RTS simulation program. This is justified by the fact that fast reaction times of the protection relays being tested completely exclude the possibility of meaningful human intervention during the simulation run.

RTS application uses standard AIX mechanisms to lock itself inside the real memory space, maps the I/O devices, and uses the interrupt disable function to suspend the operating system scheduler. The problem is further simplified by allocating a separate RISC machine for the GUI intensive operator interface.

All of the synchronization tasks are allocated to the DSP subsystem. The primary simulation clock is generated locally inside each of the 3 waveform reconstruction cabinets. This makes it possible to satisfy the tight sampling clock jitter requirements (<±1ns peak). The clock is then supplied to the DSP processors and used as a primary synchronization source.

Analysis of the application requirements reveals another interesting fact. Inability of the real-time simulation to meet the externally imposed timing constraints may not be disastrous provided that the error is reliably detected, followed by an orderly system shut down and immediate operator notification. The operator is then left with a number of options such as lowering the requested simulation sampling frequency, performing further model reduction through equivalencing, or carrying out further model optimization.

In the described simulator, the timing correctness verification function is evenly distributed to all 5 processors in the system dedicated to real-time simulation.

The data flow among processors is organized as a two way pipeline with a back pressure mechanism used to regulate the data flow. Pipeline depletion detection is used to indicate a timing constraint violation.

This approach splits the hardware system into 3 distinctive layers as shown in Figure 3.

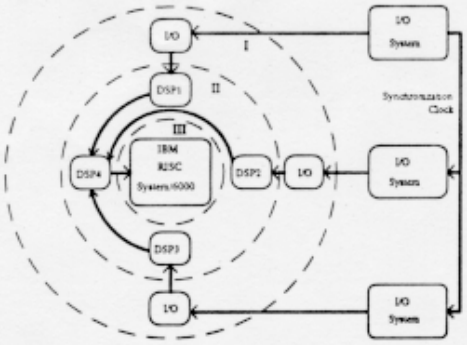

Figure 3. Organization of the Real Time System Synchronization

The first (hardware) layer is dedicated to satisfying the ±1ns sampling clock jitter requirement. The constraints are then relaxed in the second layer, enabling the DSP processors to operate with a basic 50 to 110µs clock period. The constraints for the third layer can further be relaxed by using the operating time delays inherent to the power system circuit breaker operation. The operating time of those devices is typically in the order of 16 to 80 ms. If desired, a portion of this time can be conveniently used to minimize the RTS system synchronization overhead by forming and exchanging larger data blocks between the DSP4 and the RS6000 simulation computer. This action increases processor utilization and provides additional transient load balancing.

5. Real-Time Simulator Performance Evaluation Methodology

Significant effort was invested into the simulator performance verification activity. The task was divided into the following major areas:

- RTS Modeling precision and code validation
- Real-Time system verification
- Reconstructed analog waveform precision

RTS modeling validation is performed by a series of carefully selected simulation cases. The results of RTS simulation are then compared against the ones obtained from the industry standard EMTP (ElectroMagnetic Transients Program) used for off - line studies of transients in electrical power systems. The comparison is performed by different means; from simple waveforms plotting to analysis of the signals spectra.

Real-Time system verification results are shown in Figure 4.

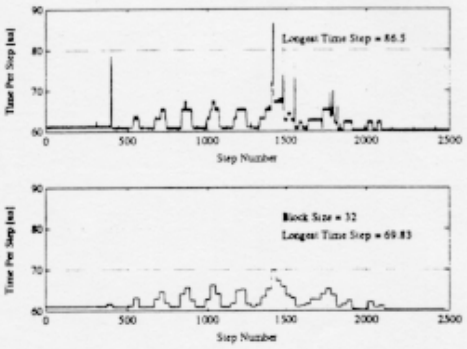

Figure 4. Real-Time System Verification Results

Upper graph shows the actual time step execution times measured during a typical RTS simulation run. Data was obtained by using externally connected event logger with 0.5µs time resolution. Logger was measuring the actual time elapsed between I/O data transfers from RISC RS6000/580 to the DSP subsystem.

As already mentioned, the system is capable of using the inherent circuit breaker operating time delays to optimize the real-time execution. Lower graph shows the simulation results indicating the worst case scenario with 32 frame block synchronization approach. As expected, the block synchronization efficiently minimizes transient computational load increase incurred by the topology updates (switch operation).

Real-time performance of the instrument transformer models was verified by adding up execution times of the instructions in the optimized, hand-crafted assembly language code. Inspection of the equivalent code produced by the TI C-compiler indicated that very substantial execution time reduction has been achieved by programming directly in the assembly language. This is partly due to the constraints imposed by the run-time

environment of the compiler generated program and partly due to limited capability of the optimizer to take full advantage of all architectural features of the TMS320C40 digital signal processor. The efficiency of the instrument transformer implementation made it possible to reduce the number of processors in the DSP subsystem and to allow reasonable time margins for communication related functions. Table II presents execution times of the single step computations for the CT implementation and two different CCVT implementations (IIR filter and circuit based, respectively). It follows that four transformer models of each type can be assigned to a single DSP chip.

Table II. Single Step Execution Times for the Instrument Transformer Implementation

Instrument Transformer	Execution Time in μs
CT	1.6
CCVT-IIR	1.0
CCVT	4.68

The reconstructed analog waveform precision is verified off line, by replaying a set of known excitation signals and measuring various aspects of reconstruction system operation. Among other things, the measurements include: output offset, gain error, frequency response, phase response, output impedance as a function of frequency, harmonic distortion, intermodulation distortion, and out of band frequency component attenuation. The offset and gain measurements are subsequently used for on-line offset and gain error correction during the actual simulation runs.

6. Conclusion

Based on the experiences related to the real-time simulator development, the following are the conclusions:

- commercially available computer hardware and system software can be utilized in designing a real-time power system simulator
- careful allocation of simulator tasks to different processors enables optimal utilization of computing resources
- special attention needs to be given to the application software where the code can be optimized to the given architecture.

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