AN ADVANCED PC-BASED DIGITAL SIMULATOR FOR PROTECTIVE RELAY TESTING

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Abstract – **This paper describes the design of a new PC-based open-loop digital simulator for relay testing. The simulator is aimed at the users that want flexibility and power of transient relay testing at a price comparable to the price of conventional test sets. The simulator can use several different I/O hardware platforms enabling the users to match simulator configuration with their testing requirements. The simulator can load and replay transient files in a variety of file formats ranging from various DFR native formats to EMTP/ATP output file formats. Test files in COMTRADE format can also be used. Various signal processing and manipulation functions of the user interface enable easy and fast test creation and execution.**

Keywords – **Digital Simulator, Protective Relaying, Transient Relay Testing, Open-Loop Testing, DFR File Replaying**

I. INTRODUCTION

Recent development of digital simulator technology has provided an opportunity for using digital simulators in testing protective relays both in closed-loop and open-loop modes [1]. As prospective users are becoming more exposed to the simulator technology, application of the simulators is gaining an increasing interest in the power industry. However, a wide acceptance is contingent upon this new technology being affordable. In most of the relay test applications this leads to a requirement that the total simulator cost does not exceed an investment required for the standard test sets. Also, some utilization of the investments made in the past into the standard test sets is desirable. This can be translated into a requirement that new digital simulators designs should be flexible to enable users to select hardware and software that fit their application requirements. According to the requirements outlined here, it is expected that most of the new simulator designs will be centered around a standard PC.

This paper describes a new digital simulator design that meets the requirements outlined above. The simulator is PC-based, yet it has the functionality of a full-blown digital simulator. This has been achieved by developing and utilizing new software for user interfacing, test signal processing and waveform replaying. To reduce the overall cost, this software does not rely on the use of external software packages, such a MATLAB, for realization of certain functions. In addition, the software is written in such a way that either the existing test sets or custom-designed, high-precision hardware can be selected as the I/O hardware. In the latter case, the additional flexibility is provided in selecting the power amplifier subsystem where either amplifiers from the standard relay test sets or high power amplifiers can be used. In order to exploit power of the electromagnetic transient simulation programs in relay testing, the simulator design also incorporates modules that enable interfacing with a variety of popular transient simulation programs. This feature significantly increases the testing capabilities of such a simulator. In addition, since some of the most popular electromagnetic transient programs and their graphical user interfaces are available for free, this can significantly reduce the overall cost of the simulator.

II. EXISTING TESTING APPROACHES

A traditional way of relay testing has been the phasor-based testing using conventional test sets. The simplicity of the test methods used and flexibility for testing applications involving relay operating characteristic as well as the portability and relatively low price of the test sets make this testing approach especially attractive. Testing with relay test sets may suit well those users that perform a lot of periodic relay tests aimed at verifying relay setting without performing extensive evaluation of the transient performance.

While this approach may be entirely sufficient for many applications and users, there may be cases that require a more thorough relay evaluation. The examples include cases when: the suitability of a particular relay to a specific application is studied; the design characteristics of a new relay design are being checked; the relay misoperations are being analyzed. The existing relay test sets can not meet these requirements and digital simulators for relay testing are used instead. Today, some manufacturers of digital simulators are offering solutions for such applications [2].

Existing simulator designs can be divided into two main categories: open-loop and closed-loop. The difference is in the way the relay under test interacts with the simulator and model of the simulated power system. With open-loop simulators, the users test relays by applying appropriate test waveforms to the relays and verifying that the relay operates in accordance with the expectations [3, 4]. The test signals are either simulated or recorded in advance. Therefore, there is no feedback from the relay to the simulation model. With this type of the simulator one can test relay operations under a variety of operating conditions including transients. On the other hand, test signals that closed-loop simulators apply to the relay under test are calculated in an on-line simulation [5-7]. The simulator can recognize a trip command issued by the relay under test and use it to immediately change the network topology of the model by opening or closing associated circuit breaker. Since the transient simulation is going on as the relay testing progresses, these simulators are also called real-time simulators. This type of simulators enables users to study more closely the relay interactions with the power system elements. Majority of today's simulators belongs to one of these two groups, but there are also some designs that combine the features of both simulator types [8].

The computer hardware used to realize simulator designs described above varies greatly [1]. Basically, one can recognize three approaches: simulators based on custom-designed computer, workstation based simulators, and PC-based simulators. Generally, the choice of the simulator computer is linked with a degree of testing functionality one wants to implement. Currently, closed-loop simulator are based either on custom-designed computers or on workstations. The open-loop simulator designs are mainly based on workstations or PCs. Having in mind the current pace of the advancements of the microprocessor technology one can expect to see more future simulator designs gravitating toward PCs.

The output hardware used to apply calculated or recorded test signals to the relay under test is also very diverse. Analog-to-digital converter subsystems are mostly custom-designed with an accent being put on the high vertical resolution and wide sampling frequency range. On the other hand, the amplifier subsystems are generally selected among various commercially available products. Their common characteristics, a high output power and wide frequency bandwidth, fit very well high-demanding relay testing applications. One possible disadvantage of this, however, is that the users that perform less-demanding applications may end up with amplifiers with broader specifications and higher prices than necessary.

As stated above, the power industry today demands more versatile and less expensive simulators. New designs are attempting to meet these demands by increasing the flexibility of the simulator output hardware and in turn widening its range of test applications.

III. NEW REQUIREMENTS

In order to meet the future relay testing requirements at a minimal cost and overcome limitations of the existing simulator designs, the following set of general design requirements was defined:

- Simulator computer should be a personal computer (PC) since the majority of test set users is familiar with this technology. Since many users already posses PCs, total investment in the simulator hardware is reduced.
- Simulator input/output hardware should be available "off the shelf" with a strong emphasis on the use of existing test sets. The additional possibility of using other high-performance output platforms is recommended.
- Simulator system software should be based on the commercially available platforms. The investment in this segment of the software should be at the lowest possible extent.
- Simulator application software should be written in a high level programming language. The horizontal and vertical portability across different platforms and within future upgrades of a given platform respectively must be on the top of the design requirement list.
- Simulator should have a simple Graphical User Interface implemented using standard graphical tools.

On the other hand, a set of the simulator design requirements related to the specifics of the relay test applications can be defined as follows:

- The simulator should operate in an open-loop mode, but future extension should also include real-time mode of operation.
- The testing of relays should be possible by applying either recorded or simulated waveforms. Most probable sources of the test waveform files are either digital fault recorders or transient simulation programs. The simulator software must be able to replay these files.
- If the test waveform files are not readily available, the simulator should provide means for their generation. The use of internal or external transient simulation programs (such as ATP/EMTP) should be a standard feature.
- An efficient user interface for the test waveform file manipulation and processing must be provided. This is needed since the recorded or calculated waveforms often can not be used without further processing to fit the characteristics of the particular test application.

To meet these requirements, a new simulator design is defined and implemented as described in the following sections.

IV. NEW DESIGN

This section describes the principal elements of the new simulator design. Only main aspects of the hardware and software architecture are elaborated on in this section, while the details and characteristics of the simulator implementation based on this design are discussed later.

A. Hardware Architecture

In accordance with the simulator design requirements, the major hardware building blocks of the simulator architecture can be represented as given in Fig. 1.

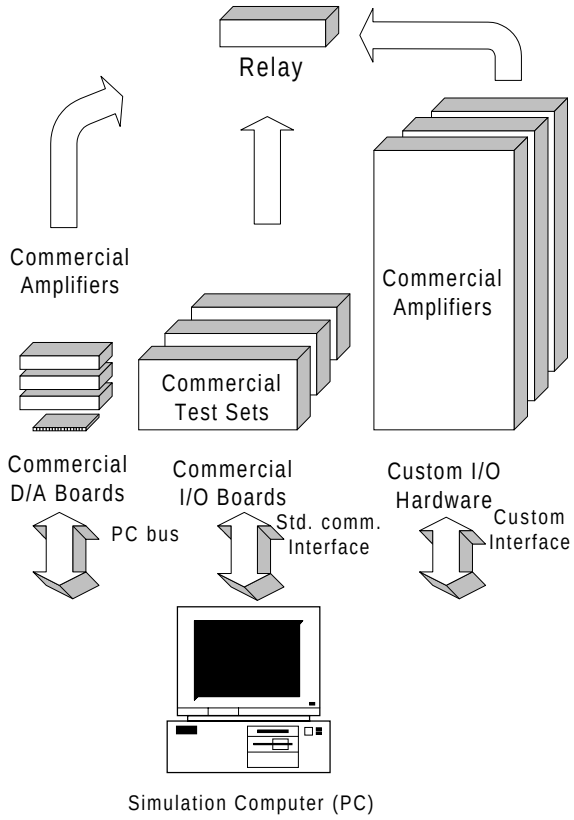

Fig. 1. The hardware architecture of the simulator

Simulator Computer

As described earlier, one of the fundamental requirements of the design is that it is based on a personal computer (PC). Generally, any PC equal or better than 80836 is acceptable, but recent Pentium models are recommended to achieve a smooth operation of the graphical user interface. Similarly, although 16-bit Windows operating system is still acceptable, Windows 95 or Windows NT are recommended. Additional factors in selecting a PC are the number of the extension slots needed for various interface cards and memory size.

Communication Interface

Depending on the choice of the output hardware for a particular simulator implementation, the simulator design may include either a custom-designed or standard communication interface.

If commercial plug-in D/A boards are used, there is no need for special communication interface since the boards are plugged directly into the PC bus. Typically, AT or PCI bus is used. On the other hand, with commercial relay test sets additional interface must be used. Typically, the choice is between GPIB and RS-232 interfaces. The communication protocols for both interfaces are well-defined. The selection of the custom-designed I/O hardware usually means that a custom-designed communication interface is also needed. Such an interface is designed for and used only with the specific I/O hardware. The communication protocols are defined accordingly.

Output Hardware

The standard test sets may prove to be the most attractive option for the majority of the test set users. The reason for that is an investment that has already been made as well as the familiarity to the majority of the users. Most relay test sets can be controlled through software allowing the developers to come up with customized software solutions. Further appeal of this option is the existence of embedded test set functions that can be utilized by the new software.

Due to the fact that the simulator hardware specifications are defined by the intended applications, custom I/O hardware may offer the best testing characteristics. The vertical resolution of a custom I/O hardware is usually higher (16 bits) than the vertical resolution of most of the relay test sets and D/A boards (12 bits). The sampling rates are also higher and signal reconstruction more sophisticated. Test signals are amplified by the commercially available power amplifiers, which offers additional hardware flexibility. The amplifiers of the test sets accepting analog inputs can be also used.

Data acquisition manufacturers today offer a great number of digital-analog conversion boards. The specifications of some of these boards fit very well the relay test requirements. Even 16-bit D/A cards with a sophisticated signal reconstruction are available at a very affordable price. When used together with commercial power amplifiers, these cards offer an opportunity for building a powerful and inexpensive relay test system hardware.

B. Software Architecture

The simulator software architecture is shown in Fig 2. The main elements of the architecture are described below, while some examples of the software implementation are left for the subsequent section.

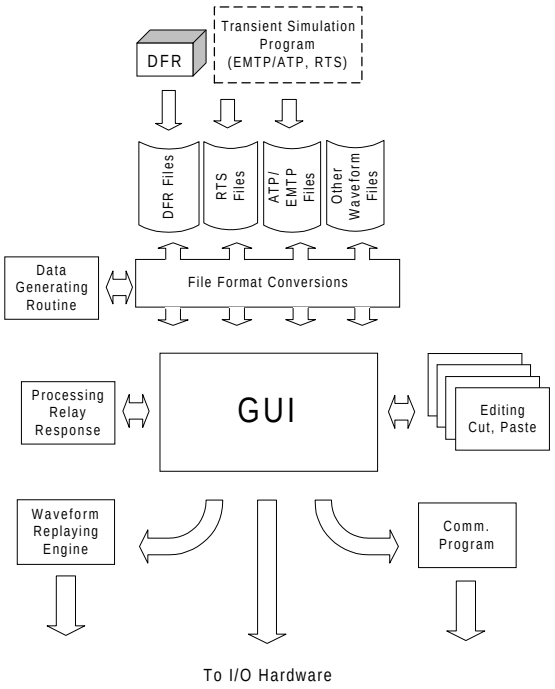

Fig. 2. The software architecture of the simulator

Data Generating

The waveform files used for testing usually originate either from digital fault recorders or from transient simulation programs. A great variety of file formats is used today and the simulator software must include a file format conversion layer to facilitate the use of the most commonly found file formats. In any case, the COMTRADE format should be a standard feature [10].

Data Manipulating

The waveform files generated by the transient simulation programs or recorded by digital fault recorders usually require certain manipulation and adjustments in order to be actually used for the testing. The routines implementing signal editing and processing functions such as cut, paste, insert, resample, rescale are examples of the functions typically supported.

User Interfacing

The graphical user interface is the single most important element of the overall software design. Its functions for test, file and waveform handling as well as, signal processing and displaying have an effect on the productivity of the simulator users. Additionally, in a flexible simulator hardware design, the graphical user interface is responsible for providing required software transparency.

Data Replaying

Prepared waveform files need to be submitted (replayed) to the relay under test through a digital to analog conversion system. Depending on the selection of the output hardware, various implementation forms of the replaying engines are available. Replaying engines accompanying custom-designed hardware exhibit greater flexibility, but they are usually the most complex and difficult to implement.

Data Processing

After replaying the waveform file, the software must assist the user in the processing of the relay response. The role of the processing is to extract as mach information as possible from the raw relay trip data. The results obtained after the processing have to be suitable for further use and analysis with various independent software packages. To facilitate this, the final test results along with the most important data describing the test case should be saved into a database.

V. IMPLEMENTATION

The characteristics of the simulator implementation are briefly presented in this section.

A. Hardware

Current PC simulator implementation supports two output hardware platform options:

Option I - Simulator using a commercial test set as the output hardware. Two-set, three-phase simulator is available for applications requiring back-to-back testing with standard output power.

Option II - Simulator using high-power amplifiers and a custom I/O interface system. Two-terminal, three- and four-phase simulators are built for most-demanding multi-terminal applications.

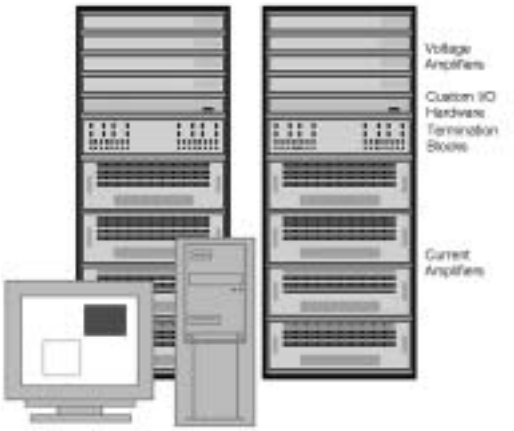

Fig. 3. PC-based simulator, hardware option II

The main characteristics of the I/O hardware for both simulator versions are listed in the table I.

Table I. I/O HARDWARE CHARACTERISTICS

Characteristic	Hardware option I	Hardware option II
Comm. interface	GPIB	Custom
Vertical resolution	13 bits	16 bits
Sampling freq.	50 μHz - 20 kHz	5 Hz - 40 kHz
Over-sampling	No	Yes
Current output	30 A rms., 150 VA	180 A peak, 1550 W
Voltage output	300 V (rms.)	120 or 300 V (rms.)
Configuration	1-, 2- or 3-phase	3- or 4-phase

B. Software

The simulator software consists of four layers:

Layer I - Software modules related to the test case creation.

These modules provide the capability of reading, processing and replaying the following waveform files: COMTRADE, ATP/EMTP, MATLAB, and native DFR files (Rochester, Hathaway). Other modules automatically invoke ATPDraw and ATP or generate the test waveforms with specified harmonic content. ATPDraw libraries of the customized power system elements tailored for relay test applications are also included in this layer.

Layer II - Software modules related to the test waveform manipulation and processing.

These modules provide test waveform editing and processing capabilities such as: cut waveform segment (e.g. to eliminate noisy part of a signal), insert waveform segment (e.g. to build the waveform from multiple segments), waveform rescaling (e.g. to decrease signal levels of replayed waveforms), waveform resampling (e.g. to decrease waveform sampling rate for EMTP/ATP generated files), waveform polarity change (e.g. to rectify wrong measuring connection), automatic pre-fault and post-fault extension (e.g. to increase the length of a DFR record), etc.

Layer III - Software modules related to graphical user interface

These modules provide facilities for the test case creating, editing and storing. The functions implemented here enable the users to visually inspect and select desired waveforms from a waveform file and save them in a test file for later replay. All processing functions mentioned earlier also have the corresponding outlets in the user interface. In addition, the modules that collect, process and store the information about relay response are also controlled from here.

Layer IV - Software modules related to the waveform replaying and collecting relay responses

This layer includes software communication modules for two possible I/O hardware platforms. A flexible waveform replaying engine used with custom I/O hardware is capable of continuously replaying very large waveform files.

The Fig. 4 shows one typical dialog of the graphical user interface. On the left side, in the tree view one can see the test elements of a test procedure currently being created. One of its elements is expanded so that defining test signals can be seen. Pop-up dialogs in the front are related to the insertion of a new test member in the test procedure. They enable the user to select and assign desired waveforms to a particular output terminal. Display view seen in the background is used for the visual signal inspection as well as for signal editing.

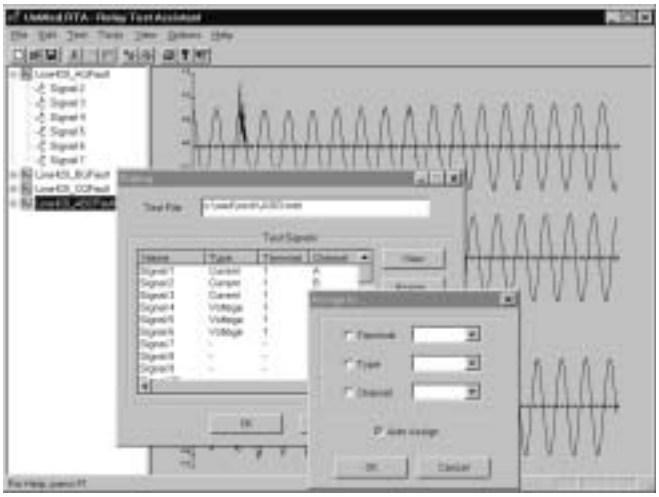

Fig. 4. The simulator graphical user interface

The simulator software has been implemented in the C/C++ [11]. The graphical user interface has been developed using Visual C++ [12].

VI. CONCLUSIONS

The digital simulators for relay testing meet most of the requirements encountered in practical relay test applications. A wide variety of simulator designs exists today enabling the users to choose a simulator that matches their testing needs. However, the wider acceptance of this technology is contingent upon its affordability.

A common practice in the utilities today is to perform the routine relay testing using conventional relay test sets. The utilities expect that any new testing technology be comparably affordable. In the past the large investments have been made into relay test sets. The requirements of the utilities is that these sets must be utilized.

To meet the requirements mentioned above, a new simulator design that offers greater hardware flexibility and less expensive implementation platforms is proposed. This simulator can utilize the output hardware of existing test sets or customized hardware solutions. The simulator software is designed and implemented using an object-oriented approach (C++) with the use of modern tools for the rapid software development (Visual C++). Thanks to this, the simulator exhibits a large degree of the hardware independence.

The main benefits that simulator design described in this paper brings to users are: the use of the existing relay test equipment and the possibility for a gradual investment into the simulator.

VII. REFERENCES

[1] M. Kezunovic, “Modular Simulators Match Cost and Performance Criteria”, IEEE Computer Applications in Power, April 1996

[2] Test Laboratories International, Inc.: “Relay Assistant - PC-Based Simulator for Open-Loop Relay Testing”, Product Brochure, 1997

[3] Kezunovic, et. al. "Advanced Signal Processing and File Management Software for Relay Testing Using Digital Simulators", 11th. PSCC, Avignon, France, September 1993.

[4] M. Kezunovic, et. al. "Design Characteristics of and Advanced Two-Terminal Digital Simulator for Relay Testing", First International Conference on Digital Simulators, College Station, Texas, April 1995.

[5] Kezunovic, et. al. "Transient Computation for Relay Testing in Real-Time", IEEE Transaction on Power Delivery, vol. 9, no. 3, July 1994, pp. 1298-1307.

[6] M. Kezunovic, et. al. "Computing Responses of Series Compensation Capacitors with MOV Protection in Real-Time", IEEE Transaction on Power Delivery, vol. 10, no. 1, Jan. 1995, pp. 244-251.

[7] M. Kezunovic, et. al. "Design, Implementation and Validation of a Real-Time Digital Simulator for Protection Relay Testing", IEEE Transaction on Power Delivery, vol. 11, no. 1, Jan. 1996, pp. 158-164.

[8] N. Izquierdo, et. al. "Digital Simulator Design for Real-Time and Open-Loop Applications", First International Conference on Digital Power System Simulators, College Station, Texas, April 1995.

[9] M. Kezunovic, et. al. "Extensible Graphical User Interface for Digital Simulators", First International Conference on Digital Power System Simulators, College Station, Texas, April 1995.

[10] Revision of C37-111 (COMTRADE) Standard, IEEE Power Engineering Society, Power System Relaying Committee, December 1996

[11] B. Stroustrup, The C++ Programming Language, Second Edition, Addison-Wesley Publishing Company, 1991

[12] D. Kruglinski, “Inside Visual C++”, Microsoft Press, Third Edition, 1995

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